

Scalable synthesis and device integration of self-registered one-dimensional zinc oxide nanostructures and related materials

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Babak Nikoobakht,^{*a} Xudong Wang,^{*b} Andrew Herzing^a and Jian Shi^b

On integrating one-dimensional (1D) nanocrystals (nanowires) to useful devices, in this review article, we provide a background on vapor-based growth processes and how they impact device integration strategies. Successful integration of nanowires to devices and their scalability simply rely on where and how nanowires are formed, how they are interfaced to other device components and how they function. In this direction, we will provide a discussion on developed growth strategies for lateral and standing growth of semiconductor nanostructures and assess their success in addressing current challenges of nanotechnology such as mass integration of nanowires, and the necessary accuracy in their positioning and alignment. In this regard, we highlight some of our recent work on formation of two-dimensional (2D)- and three-dimensional (3D)- nanowire and nanowall arrays and provide an overview of their structural and electro-optical properties. This will be followed by discussing potential applications of such hierarchical assemblies in light generation, photocatalysis and conversion of motion to electricity.

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1. Introduction

Optical lithography continues to be the most prevalent technique for further miniaturization of electronic circuitry and its components. However, as device miniaturization continues, both complexity of pattern generation and its cost increase,¹ limiting the use of such techniques to high-end applications, such as micro-processor manufacturing. As an alternative, nanomaterials and

^a Surface and Microanalysis Science Division, 100 Bureau Dr Stop 8372, National Institute of Standards and Technology, Gaithersburg, MD, USA 20899.
E-mail: babakn@nist.gov; Fax: +1 30 1926 6689; Tel: +1 30 19753230

^b Materials Science and Engineering Department, University of Wisconsin-Madison, Madison, WI, USA 53706. E-mail: xudong@engr.wisc.edu; Fax: +1 608 262 8353; Tel: +1 608 890 2667



Babak Nikoobakht

Babak Nikoobakht is a physical chemist at the Material Measurement Laboratory of the National Institute of Standards and Technology in Gaithersburg, MD. He also holds an adjunct faculty position at the chemistry and biochemistry department of University of Maryland-College Park. He received his PhD from Georgia Institute of Technology in 2002. His research interests include anisotropic growth of nanocrystals and exploring

relation between structure, property and function of ensemble of one-dimensional nanocrystals.



Xudong Wang

Dr Xudong Wang is an assistant professor in the department of Materials Science and Engineering at University of Wisconsin – Madison. He received his PhD degree from Georgia Tech in 2005. His current research interests include studying the growth and assembly of oxide nanostructures for mechanical and solar energy harvesting, and understanding the coupling effect of semiconductor properties and piezoelectric polarization.

non-conventional nanofabrication methods such as “bottom-up” chemical approaches could offer platforms to fill the technological gaps with potential advantages in terms of performance and/or cost.

Foreseen for many applications, the expected function of a nanostructure in a given device is not the only specification on the quality assurance check list. There are other requirements including structural and performance reliabilities that must be understood and modeled in order for the nanodevice to be considered industrially and commercially viable. In this regard, mass interfacing of semiconductor nanostructures with other semiconductors or metals remains among the technical barriers that must be addressed for realization of platforms that enable control over circuit topology and devices therein. Furthermore, chemical, physical and structural properties of these junctions as well as the device functions must be predictable.

In this review article, we provide readers an account on the progress, challenges and underlying problems in developing useful architectures for nanodevice fabrication *via* vapor deposition techniques. This overview also provides examples on popular semiconductor oxides such as ZnO and TiO₂ and discusses important elements needed in the process of materials design to device innovation, though, the underlying emphasis remains on the directed assembly and interfacing of 1D-nanostructures. This is an important topic, which has to be addressed in any nanowire device integration regardless of the nanowire growth method. The evaluation of candidate materials, their applications and the critical issues related to producing practical devices, both in planar and free-standing formats will be discussed as well.

2. Significance of 1D-semiconductors and the need for alignment techniques

1D-nanostructures share some common characteristics with their 0D- and 2D- counterparts, such as quantum size effects, but geometrically offer advantages that are absent or difficult to

realize using the other two categories.² By definition, nanowires offer a unique combination of dimensionality, where the longitudinal direction exceeds hundreds of nanometers or even micrometers in length while the transverse direction is confined to a few tens of nanometers or less. Since the former is accessible using current microfabrication techniques, the topographies and architectures of nanowire-based devices offer the potential for probing materials at the sub-100 nm dimension.

In addition, due to their larger surface area, they are more susceptible in sensing the variation in their immediate surroundings. This has led to realization of novel platforms, for instance, in biosensing.³ 2D-film growth typically requires cumbersome growth chambers while high quality nanowires can be formed using inexpensive vapor phase transport or solution-based methods. As discussed in the following sections, nanowires offer the ability to form unconventional crystals, *e.g.*, by extending their anisotropic growth to a 3D network such as hyperbranched nanowires. Using such nanosystems, it is also possible to realize crystal facets that are not thermodynamically observable in thin films; for instance, the formation of non-polar facets in wurtzite crystals important in light emitting devices. Other benefits exhibited by nanowires, compared to a 2D film, could include more degrees of freedom in managing their defects, lattice constant, lattice strain, and doping profile. Owing to their small volume and interfacial areas, the above properties are expected to result in novel material combinations and device concepts.

Some of the earliest reports on the growth of nanowires or whiskers dates back to the 1960s^{4,5} and 1970s.^{6–8} However, research on 1D-nanostructures was limited until the late 1990s boom of research on this topic,^{9–11} perhaps due to the rise in demand for alternative nanosystems to silicon microelectronics. Nowadays, research on nanowires has deeply penetrated various disciplines including chemistry, materials science, physics, biology and engineering with emerging applications in clean energy, sensors, catalysis, electronics and digital displays.



Andrew Herzing

Gaithersburg, MD. Currently a staff scientist in NIST's Material Measurement Laboratory, he is developing techniques to enable the structural and chemical analysis of nanomaterials at ultrahigh spatial resolution.

Andrew Herzing received his PhD in Materials Science from Lehigh University in 2007 under the supervision of Prof. Christopher Kiely. He was subsequently awarded a National Research Council postdoctoral fellowship to study the nano- and atomic-scale characterization of materials using transmission electron microscopy and microanalysis techniques at the National Institute of Standards and Technology (NIST) in



Jian Shi

nanomaterials, photovoltaics, photoelectrochemical cells, nanogenerators and piezotronics.

Jian Shi obtained his BS degree in Materials Science and Engineering at Xi'an Jiaotong University in 2006, MS Degree in Mechanical Engineering at the University of Missouri-Columbia in 2008, and is currently finishing his PhD degree under the supervision of Prof. Xudong Wang in Materials Science Program at the University of Wisconsin-Madison. His research focuses on the nucleation and growth of oxide

One of the fundamental challenges in integrating free-standing semiconductor nanowires with the highly ordered components of an electro-optical or electro-mechanical device is being able to control the overall hierarchy of nanowires either in planar or standing format.^{12–14} Another issue is how to accurately position the active area of the individual nanowires between the necessary electrodes within a device. An ideal method for controlling these parameters should enable the reproducible placement of nanowires on a large scale such that their position and orientation are predictable. In recent years, several methods have been devised for incorporating free-standing nanowires into *planar* devices. The common feature in these methods is the need for a substrate to receive the nanowires and an external force to drive the transfer and alignment of nanowires onto this substrate. A variety of driving forces such as capillary forces,^{15,16} shear stress,¹⁷ adhesion forces,^{18–20} inertial forces²¹ and nanopatterning^{18,22} have been utilized to control the orientation of an ensemble of nanowires on a given surface. Among them, nanoimprint lithography and pattern transfer techniques^{23,24} demonstrate the most promise in terms of precision and control. However, their use becomes challenging and costly as the relevant object sizes drop below 100 nm or as nanoobject number per site is reduced. Overall, current technologies are more suited to the collective integration of monolayers of nanowires with devices; for instance, in flexible electronics,²⁵ transistors,¹³ and sensory applications.¹² For applications that require electrically addressing single or small groups of nanowires in a scalable fashion, the inherent uncertainties of the available techniques make them incapable of competing with top-down strategies for the realization of complex architectures and circuitries.

3. Growth mechanisms of nanowires and challenges in scalable interfacing

In general the synthesis of nanowires can be classified into two groups of growth processes: metal-catalyzed, and metal-free⁷ that can take place in solution and in the gas phase. In the first group, also known as vapour–liquid–solid (VLS), vapor–solid–solid (VSS) and solution–liquid–solid (SLS) growth techniques, a metal catalyst acting as a nanoscale solution, dissolves the incoming semiconductor precursors from the gaseous (or solution) phase and confines the nanocrystal growth, resulting in the formation of free-standing nanowires. Such nanowires can typically be distinguished from those produced *via* other growth processes by the observation of a solidified droplet at their tip. In contrast, metal-free nanowire growth is generally considered to be a vapor–solid (VS) or solution–solid (SS) growth process. Among the factors that are known to initiate this type of growth are surface defects in the substrate such as impurities or screw-type dislocations.^{7,26} In addition, imbalances in the stoichiometric ratio of the precursors during crystal growth could also result in precipitation of an excess component on some crystal facets, thus stimulating the VS or SS growth.²⁷ In solution phase, nanowires are generally grown in colloidal form^{28,29} or on a solid surface.^{30,31} In this case, analogues to the VS growth, nucleation sites are typically necessary to initiate the growth. Examples include growth of ZnO or TiO₂ nanowires in

which a seed layer is first deposited on the surface of interest to start the growth. Similar to gas phase techniques, this method is also shown to be capable of forming well-aligned and high quality free-standing nanowires^{32–34} with applications in hydrogen generation,³⁵ dye-sensitized solar cells,³⁶ and energy generation.³⁷

Site selectivity of the growth in both gas phase and solution phase methods have been controlled using natural surface defects such as screw dislocations of the underlying substrate²⁶ or using surface patterning techniques. Although the first approach is inherently scalable, its main drawback is the lack of site specificity. The surface patterning can predictably control the position of the nanowires and has been shown on small scales *via* high resolution patterning,³⁸ and on larger scales using interference photolithography.³⁹ Masking a surface with 1D nanopatterns has also been used for horizontal growth of nanowires in which they are either grown nearly parallel to the surface, but in a suspended form,³⁷ or grown laterally in full-contact with the substrate.²² In the latter group of approaches, the width of the opening in the mask determines the nanowire width. As such, to grow small diameter nanostructures, it becomes necessary to use high resolution lithography for nanopattern generation.²²

ZnO and TiO₂ are the two most intensively studied semiconductor oxide materials and many of their methods of synthesis have been successfully applied for 1D-growth of other nanostructures such as SnO₂ (catalytic VLS, Molecular Beam Epitaxy, Pulsed Laser Deposition),^{40–43} V₂O₅ (thermal evaporation, hydrothermal, sol-gel and electrodeposition),^{44–47} WO₃ (CVD, hydrothermal, electrodeposition),^{48–50} and Fe₂O₃ (CVD, flame synthesis).^{51–53} As it can be seen, nanowire growth strategies including VLS, SLS, VS or SS are well-developed and offer unique capabilities such as simplicity, scalability, site specificity, control over composition and control over morphology. These methods can be utilized separately or combined to prepare nanostructures with unprecedented form factors such as homo- and heterojunctions, tubular quantum wells, and shells with axial or radial configurations.^{54–62} Diversity in device shape is one of the unique distinctions of 1D-nanocrystals that cannot be achieved in 2D-films due to geometrical constraints.

In interfacing nanowires, it is the nature of an application or a device function that determines the method of integration and the necessary hierarchy of nanowires in a device. For instance, if a 2D-network of nanowires is needed to form an electrically conductive layer, then control over the registration of the nanowires may not be as important as their electrical connectivity within the network. However, if the application requires charge transport through a single nanowire or a particular group of nanowires, without intercepting each other, then control over their relative position and orientation becomes crucial. One of the existing challenges is that most of the methods highlighted above yield randomly distributed nanowire networks which their interfacing to outside world is a daunting task. One quick fix to this limitation has been the use of bulk of nanowires in randomly distributed nanowire networks, however, this arrangement typically do not exhibit the performance of original nanowires.

In addition to the use of alignment techniques discussed in Section 2 for building 2D- or 3D-nanoarchitectures, intrinsic

structural relationship between a substrate and nanowires can be used to control their overall hierarchy. These approaches naturally enable control of the organization of nanostructures on a wafer scale, leading to more facile device integration. One of the requirements of this methodology is the ability to predictably guide the growth of 1D-nanostructure from a specific site and facet. In the following sections the focus is given to the mutual interactions between substrate and nanowires and factors that guide the nanocrystal growth on or from a single crystal substrate. Well known examples of these processes are free-standing and lateral growth of semiconductor nanowires, which are discussed in the following sections.

3.1 In-plane and out-of plane directed growth of nanowires

The anisotropy of a crystal, in general, is a result of the varying growth kinetics of different crystal faces. One of the fundamental needs in anisotropic crystal growth is the development of methods to selectively grow a nanocrystal facet in a certain direction. Free-standing nanowires are great examples of this as growth occurs only along a selective facet, and thus in a specific crystallographic direction. The particular direction in which a given nanowire will grow is strongly influenced by the crystal structure of the nanowire itself, as well as by the surface free-energy of the metal and semiconductor interface. For example, nanowires with cubic structures typically grow in the $\langle 111 \rangle$ direction, while those with wurtzite-type crystal structure tend to grow in the $\langle 001 \rangle$ direction.⁶³ The substrate is also considered one of the factors determining the growth direction of free-standing nanowires. In the case of lattice matched epitaxies, they can be chosen to guide the growth in a direction which is either normal to or inclined with respect to the surface; for instance, the growth of Si nanowires on a Si (001) substrate, which takes place in the $\langle 111 \rangle$ direction.¹¹ Even in lattice mismatched systems, it has been shown that the substrate impacts the growth direction of the nanowires. Examples include the preference for epitaxial and upright growth of InAs and InP nanowires to occur in the $\langle 111 \rangle$ directions on a Si (111) surface. As the diameter of such nanowires increases, population of the tilted nanowires increases, most likely to reduce the misfit strain between the two crystals.⁶⁴ In these examples, the growth is no longer epitaxial above a critical diameter due to the increase in strain energy at the interface and the formation of misfit dislocations.⁶⁵

In addition to the role played by the substrate, the interfacial energy and surface tension from the edge of the interface between the metal catalyst and a nanowire are found to be important factors in determining the growth direction of nanowires. In the case of Si nanowires, as the diameter increases the plane of growth changes in order to lower the interface energies between metal catalyst and the semiconductor.^{66,67} For instance, the growth direction of a population of nanowires has been shown to change from the $\langle 111 \rangle$ to the $\langle 110 \rangle$ direction as their diameter increases above 20 nm.⁶⁸ Other factors affecting the diversity in nanowire growth directions include the growth temperature, concentration of precursors in the gas phase¹¹ and degree of the supersaturation inside the metal catalyst.⁶³ Although the origin of the multiplicity of nanowire growth direction is fairly well understood, factors that

can selectively initiate or abort growth of a specific facet remain elusive. In this regard, we will discuss how the inherent information present on the surface of a single crystal substrate has been utilized as a scaffold to promote growth of 1D- and 2D-epilayers of other materials. This is followed by a discussion on weaknesses and strengths of available approaches in planar growth of nanowires with higher precision and predictability.

Reports on the planar or lateral growth of 1D-nanostructures have been very limited relative to those focused on free standing nanowires. The planar growth can be linked to the original work on the self-assembled epitaxial growth of quantum dots, where epitaxially grown films undergo a transformation to arrays of 3D islands.⁶⁹ The island formation is typically accompanied by generation of misfit dislocations depending on the extent of lattice mismatch. In the case of Ge on Si ($\approx 4\%$ lattice mismatch), Eaglesham and Cerullo discovered dislocation-free island formation at the expense of elastic deformation of the surrounding substrate. As the islands are overgrown above a critical thickness, misfit dislocations appear as a stress-relief mechanism.⁷⁰ If the stress is anisotropic, as in the case of Ge on Si, the island aligns itself perpendicularly to the direction of maximum stress. As the lattice mismatch increases, the anisotropy in the island shape becomes more pronounced. Anisotropy in crystal lattice match on a cubic substrate, such as silicon, has been used to transform thin films of rare earth silicides into metal silicide nanowires under a thermal annealing process. As a result of this heat treatment metal silicide nanowires are formed that are approximately 1 μm in length and 2 nm in height.⁷¹ Such growth methods typically require dissociation and reconstruction of surface deposited atoms on the heated silicon surface in order to drive the formation of nanowires or quantum wires. In these cases, as the lattice mismatch along the width of the nanowires increases, both the width and height of the nanowires tends to decrease.⁷² The width distribution of such nanowires is very broad indicating that their formation takes place far from equilibrium. In most of these cases, nanowires tend to grow from both ends and nucleate in closely-spaced groups, with no control over their location or orientation.

Lateral growth of nanowires is also shown to be driven by anisotropy in surface energy⁷³ and symmetry breakdown of the underlying substrate.⁷⁴ In the latter approach, also called “endotaxial” growth, transition metals are deposited on a Si surface at elevated temperatures. The epitaxial growth of nanowires continues into the substrate such that two of their long facets become embedded in the underlying silicon. The anisotropy driving the nanowire shape has been attributed to the varying growth rates of the nanowire end facets *versus* its embedded side facets. This synthetic route is applicable to a variety of transition metals, but lacks the necessary control of the overall nanowire morphology. Lower temperatures have been used to increase the aspect ratio of the resulting nanowires, but this also increases the nucleation sites, *i.e.*, their surface density, which decreases their spacing.⁷⁵

Self-organization of 1D-nanostructures has been also shown using surface defects or structures on a single crystal surface. These approaches can be considered part of the graphoepitaxy methodologies (*a.k.a* artificial epitaxy) in which artificial micro-patterns on a surface are used for growth of oriented crystals.

Developed in the early 1970s, this approach was originally proposed for epitaxial thin film growth on amorphous surfaces.⁷⁶ The created surface patterns must have a symmetry analogous to that of the material to be crystallized on the surface.⁷⁶ For anisotropic nanostructure growth, single crystal surfaces decorated with surface reconstructions or atomic steps have been used in order to control the directionality or alignment of the grown 1D-nanostructures. Examples include the use of arrays of Al atom of *a*-plane sapphire,⁷⁷ atomic steps⁷⁸ for the alignment of single-walled carbon nanotubes, or the growth of Ge nanowires on step defects on a silicon (113) substrate.⁷⁹ These approaches offer low-level control of orientation of the resulting nanowires in the formed hierarchy. However, they do not allow for any control over the reproducibility of the surface nanopatterns. The use of arrangement of atoms on a crystal surface potentially is one of the ultimate mechanisms to precisely guide 1D-planar growth; however, the homogeneity of substrate surface energy causes the overgrown islands to lack site-specificity and thus grow randomly. To break this surface degeneracy, metal nanodroplets used in the VLS growth process are found to be very unique, as they precisely define the nucleation sites and confine the nanocrystals growth.

3.2 Surface-directed growth of nanowires

The surface-directed vapour–liquid–solid (SVLS) growth process is nearly identical to the VLS growth of standing nanowires. In the latter, a metal nanodroplet as a solution captures the incoming precursors from the gas phase, reaches a state of supersaturation, and allows precipitation of a semiconductor nanocrystal on the substrate. The metal nanodroplet positioned atop the formed resulting nanocrystal gradually grows upward.^{5,7} In the SVLS process, the metal nanodroplet partially wets the semiconductor nanocrystal and also forms an interface with the substrate. Continuation of this process results in the lateral growth of a semiconductor nanocrystal in a specific direction with the metal nanodroplet at the leading end of the nanowire.^{80,81}

The SVLS growth of nanowires was first observed for ZnO when the spacing between Au catalyst particles was increased to distances several times larger than their size (≤ 20 nm).⁸² Later, this growth was shown to occur for Au nanodroplets formed at the perimeter of any 2D Au pattern (Fig. 1a). The tendency of the side nanodroplets to form horizontal nanowires is believed to originate from their high mobility at growth temperature of ≈ 900 °C and their volume increase due to the incoming flux of Zn and O precursors. These factors increase the likelihood of coalescence of the interior Au nanodroplets with the neighbouring ones leading to the formation of free standing nanowires.^{3,7} As a consequence of this natural selection, the Au nanodroplets at the periphery of the pattern have the opportunity to move laterally on the substrate, catalysing the growth of horizontal nanowires (Fig. 1b). Therefore, for a deposited metal pattern with a given width, both standing and horizontal nanowires are formed.

A variety of metal catalysts including Au,⁵ Ag,⁸³ Ni,⁸⁴ Cu,⁸⁵ Sn,⁸⁶ and Fe⁸⁴ have been used for growth of nanowires using the VLS and VS processes.⁸⁷ Depending on the application, the proper selection of the metal catalyst is crucial, as it significantly impacts the electronic structure of the nanowires as well as their morphology.⁸³

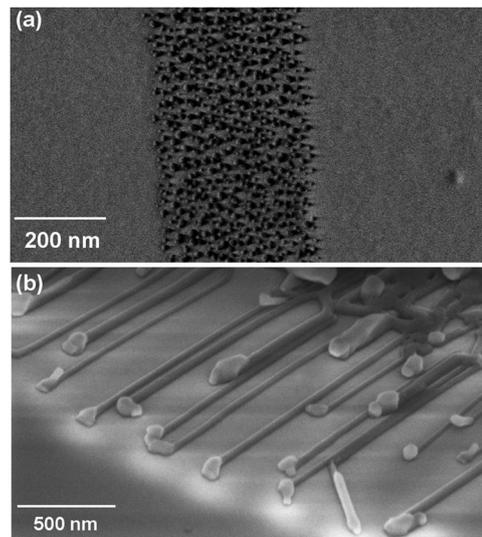


Fig. 1 Lateral growth of horizontal nanowires from Au catalyst at 900 °C in a tube furnace. (a) Part of a 10 nm-thick Au pattern annealed at 700 °C shows the arrangement of the metal nanodroplets prior to growth process. (b) Oblique view of horizontally grown ZnO nanowires from an Au pattern. After the growth, Au nanodroplets at the center form free-standing nanowires and those at the edges of the pattern result in horizontal nanowires.

In the case of ZnO nanowires, it is shown that the use of iron catalyst results in a faster growth rate, but it also induces more oxygen vacancies. Our results also indicate that the Au catalyst is found to be a superior choice compared to Ag and Cu, because Ag tends to evaporate during the high temperature growth and Cu could result in the formation of deep-level impurities.⁸⁸ However, in the VLS growth of Si nanowires, a reverse trend has been observed, *i.e.*, Au is found to result in formation of deep-level impurities, and Cu metal shows a less deteriorating effect on the resulting optical properties of nanowires.⁸⁹

In addition to ZnO, in recent years, the SVLS growth has been demonstrated for other II–VI and III–V semiconductors. Examples include the growth of GaAs,⁸¹ GaN,^{90,91} In₂O₃,⁹² and Mg₂SiO₄,⁹³ nanowires on substrates such as GaAs, GaN, sapphire and silicon. To better illustrate the directed growth process, consider sapphire, a trigonal/rhombohedral crystal in the hexagonal crystal family with unit cell dimensions of $a = b = 0.4795$ nm and $c = 1.3099$ nm. As illustrated in Fig. 2, this crystal has an elongated unit cell along its *c* axis. When zinc oxide, a hexagonal crystal with unit cell dimensions of $a = b = 0.3249$ nm and $c = 0.5205$ nm, is grown on sapphire, horizontal growth is only observed on certain facets such as the *a*-plane.⁸² Interestingly, the long dimension of the sapphire unit cell (1.3099 nm) is almost 4 times the ZnO “*a*” dimension (0.3249 nm), demonstrating a pseudo-lattice match of about 0.8%. This relationship has been accounted for the aligned growth of ZnO in the case of free standing nanowires and uniaxial epitaxy of ZnO films on *a*-sapphire.^{94,95}

The horizontal growth of ZnO nanowires takes place in $[1\bar{1}00]$ direction, which is also parallel to the $[1100]$ direction of the sapphire crystal (Fig. 2). This direction is strictly observed in the majority of the performed growth trials. However, results indicate that the number of growth directions can change at

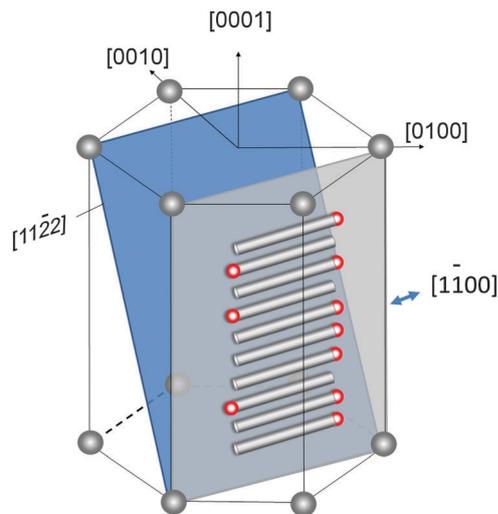


Fig. 2 Hexagonal crystal structure of sapphire and orientation of its *a*-plane with respect to the [0001] direction. Horizontal ZnO nanowires grow on the *a*-plane in the $[1\bar{1}00]$ direction.

least within the confines of the crystal symmetry of the substrate. As an example, if ZnO nanowires are grown on a GaN substrate, the growth occurs in multiple directions with a 6-fold symmetry (Fig. 3a).⁹⁶ In this case, the lattice mismatch between ZnO and GaN, in their $[1\bar{1}00]$, is only $\approx 1.8\%$, in contrast to the 32%-lattice mismatch between ZnO and sapphire; thus the nanocrystal growth is less restricted on GaN. Replacing GaN substrate with (100) silicon results in laterally grown nanowires, but with no clear directionality preference as seen in Fig. 3b. The lack of directionality could be attributed to multiple factors

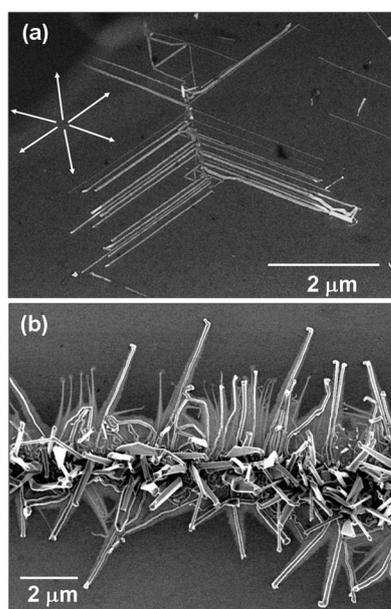


Fig. 3 Impact of the substrate on directionality of horizontally grown nanowires. (a) ZnO nanowires grown on (0001) GaN illustrate multiple growth directions with a 6-fold symmetry; while on a (001) silicon substrate (b) nanowires show no clear directionality.

including: (1) existence of the native silicon oxide layer between Si and ZnO during the growth process; (2) 3% lattice mismatch between ZnO ($a = 0.3249$ nm) and Si ($a = b = c = 0.5381$ nm); (3) difference in crystal symmetries, *i.e.*, cubic crystal symmetry of Si versus hexagonal crystal symmetry of ZnO. In growth of horizontal Mg_2SiO_4 nanowires on silicon, a 1 nm thin amorphous layer is observed at the interface, but it does not obstruct the influence of the substrate on the growth direction and despite $\approx 5\%$ lattice mismatch the epitaxial growth continues following the symmetries of both cubic crystals.⁹³ The influence of the substrate symmetry and epitaxial growth can be overridden by using artificial surface steps and grooves. In this regard it is shown that the fabricated nanosteps on a *c*-plane sapphire can force the GaN nanowires to grow along the steps and not those directions predicted by the hexagonal symmetries of both crystals.⁹¹ Another example highlighting the significance of this relationship can be understood from Fig. 4. This figure shows TiO_2 nanowires grown on a GaN substrate that has been patterned with 10 nm-thick Au features. These nanowires are carbothermally grown from TiO_2 powder (anatase phase) and as shown in Fig. 4a, demonstrate a growth direction similar to that of ZnO on GaN, *i.e.*, $[1\bar{1}00]$ direction. Based on the selected area electron diffraction (SAED) patterns in Fig. 4b, the atomic packing in the TiO_2 has a hexagonal structure (ABAB); however, there is a 30° crystal rotation in the TiO_2 diffraction spots (highlighted with arrows), which is not observed in the ED pattern of ZnO nanowires in Fig. 4c.⁹⁷

The directed planar growth of nanocrystals, based on the available models for anisotropic nanocrystal growth, can be explained by the existence of an asymmetric lattice match between

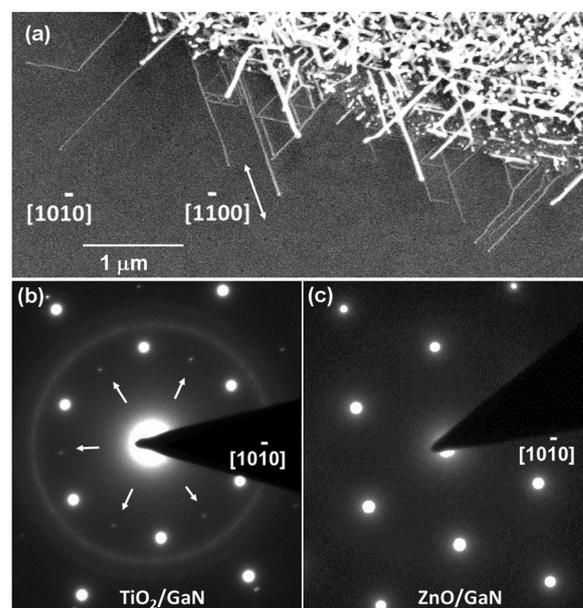


Fig. 4 (a) Horizontal TiO_2 nanowires grown from Au patterns on (0001) GaN. The highlighted crystallographic axes coincide with two growth directions. (b) SAED pattern of TiO_2 nanowires on GaN. (c) SAED pattern of ZnO nanowires on GaN. Both patterns are collected at the [0001] zone axis. The diffraction spots shown with arrows in (b) indicate a 30° rotation in the crystal orientation for TiO_2 with respect to ZnO.

the epilayer and the host substrate.⁷¹ Based on this model, the observed nanowire growth directions in the SVLS process could be indicative of the presence of high lattice match pathways between the two crystals. However, the presence of these preferred directions cannot be supported by the aforementioned examples as they include highly matched (1.8% mismatch in ZnO and GaN) and highly mismatched crystals (75% mismatch in *c*-plane ZnO on *a*-plane sapphire). As such, the results indicate a loose dependence between crystal lattice match and the directionality of the lateral growth. On the other hand, the crystal symmetry of the two crystals seems to be more influential in defining the number of growth directions.

Examination of the interface between ZnO nanowires and the sapphire substrate by high-resolution transmission electron microscopy (HR-TEM) reveals a large compressive strain in the substrate. The representative image in Fig. 5a shows the deformation of the interface due to this strain.⁹⁸ This observation opposes the existence of low strain paths along the growth directions according to the model above.⁹⁸ In the better matched case of ZnO on GaN, this stress is significantly reduced when viewed from the cross-section (Fig. 5b); however, from top view, when their *c*-planes are overlapped, no lattice match in any crystallographic direction is observed.⁹⁹ Instead a local lattice match is observed, where its coherency is maintained over a range of a few nanometers.⁹⁹ This means that a ZnO island can be formed epitaxially, but its epitaxial elongation is constrained due to the absence of a long-range lattice

match with the substrate. This contradiction can be resolved by treating the SVLS process as a sequential island growth mechanism. At the early stage of the growth, a ZnO island¹⁰⁰ is first formed at the interface between the Au nanodroplet and the substrate (Fig. 5c). As seen, the ZnO island with a hexagonal structure contains a (0001) polar face that is typically surrounded by six side facets. As explained later, results indicate that the Au droplet most likely wets half the sides of the ZnO island, which in Fig. 5c are under the Au. Two of these side facets can be seen in the HR-TEM cross-sectional image of Fig. 5b. Based on the SAED pattern in Fig. 5d, the side facets are (11 $\bar{2}$ 2) that are about 32° tilted with respect to the ZnO *a*-plane (Fig. 2). The horizontal nanowires tend to exhibit triangular cross-sections that become trapezoidal due to the presence of a (0001) facet. Both SEM and the studied cross-sections (Fig. 5b) show that the (0001) polar facet has a smaller surface area than the side facets. This may explain why an Au nanodroplet prefers migrating to side facet(s) instead of preferentially wetting the top polar facet. The Au nanodroplet also stays partially in contact with the GaN surface, which enables nucleation of the 2nd ZnO island. Repetition of the serial island growth eventually leads to the elongation of the ZnO nanocrystal in $\pm[0110]$ direction, a characteristic that is not naturally observed for ZnO nanowires and other hexagonal crystals. HRTEM cross-sectional microscopy shows a rippled nanowire surface, which most likely mean a subtle increase and decrease in height of the nanowire as the Au droplet moves forward.⁹⁹ This fluctuation in height could infer an inflation and deflation of the Au nanodroplet most likely due to build-up and depletion of the ZnO in the Au nanodroplet solution, respectively. This effect can be better observed in larger diameter nanowires *via* scanning electron microscopy (SEM) as illustrated in Fig. 6a. The zigzag structure further shows the impact of variation in the Au droplet volume on the nanowire surface. In Fig. 6b, the red solid and dash lines in the first drawing represent the Au droplet borderlines before and after its inflation due to ZnO build-up, respectively; by continuing the growth, the inflated Au droplet leaves behind a ZnO nanocrystal and shrinks in size. From SEM observations it can also be inferred that the Au droplet interfaces with three adjacent non-polar ZnO facets among which the contact with the left and right facets are partial. As the Au droplet increases (decreases) in volume its interface with these two facets increases (decreases) leading to the appearance of (11 $\bar{2}$ 2) facets. The size of these facets remains proportional to the change in Au droplet volume, which seems to be small. Despite the sequential growth, examining the crystal structure of nanowires and SAED patterns along their length (Fig. 6c) shows that the ZnO is single crystalline. In Fig. 6a, the observed structural deformation seen in the top nanowire (its right side) is due to the merge of its Au droplet with another one during its surface travel.

Our results as well as others demonstrate that the directionality of nanowires in the SVLS process is a universal characteristic and can be predictable. It is of great interest to be able to selectively control the growth rate of these facets for realization of desired nanostructures. As described above, the shape of the initial semiconductor island is a crucial factor in defining the fate of a nanostructure's morphology; it largely determines other basic characteristics such as facet growth, droplet position, and

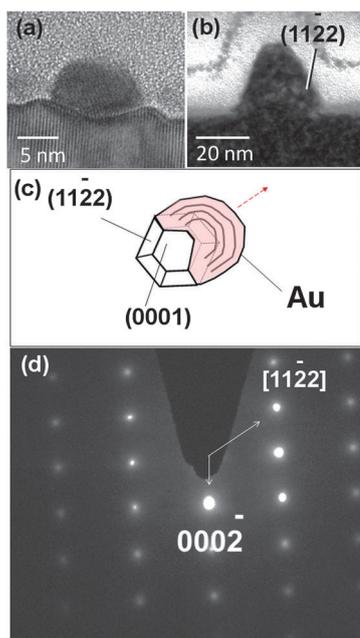


Fig. 5 Surface and interface morphologies of ZnO nanowires on sapphire and GaN. (a) Cross-section of a ZnO nanowire on *a*-sapphire. Sapphire deforms underneath the nanowire. (b) Cross-section of a ZnO nanowire on GaN. Here with a better lattice match, substrate deformation is not detectable. (c) The top view schematic of the initial ZnO island is expected to have six non-polar (11 $\bar{2}$ 2) facets. Au interfaces with three of these side facets from which the middle one has a higher growth rate determining the direction of the nanowire (red arrow). (d) SAED pattern of the nanowire segment in part (b) shows [0002] and [11 $\bar{2}$ 2] directions of the nanowire and GaN.

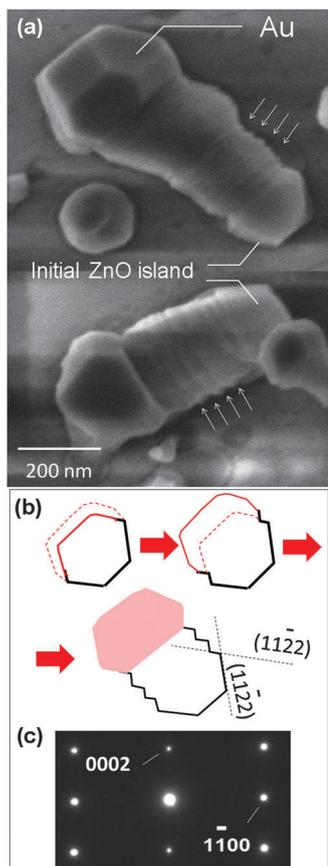


Fig. 6 (a) Surface morphology of large diameter ZnO nanowires. The nanowire includes a large segment which is the initial ZnO island with a hexagonal shape (see Fig. 5c). During the growth a fine zigzag structure is formed that is attributed to the dynamic of Au droplet motion. (b) Schematic shows three snapshots of the nanowire growth from top view. Solid red line shows the borderline of the Au droplet after formation of a ZnO island. Influx of Zn and O inflates the Au droplet border to the dash line position. Diameter of the nanowire complies with the size of the Au droplet forming the observed shape. (c) SAED pattern along the length of a nanowire shows a single crystal structure.

formation of new facets. These elementary processes have also been proposed and used by Tersoff *et al.* to model and predict the different morphologies of nanowires.¹⁰¹ In this regard, we will discuss the use of some mechanisms to further tailor the overall morphologies of assemblies of nanowires.

3.2.1 CONTROLLING AND ENGINEERING THE ORIENTATION OF NANOWIRES IN LARGE SIZE ASSEMBLIES. In addition to being able to predict the growth direction of nanowires, it is important to formulate methods to alter their preferred growth directions. One way to achieve this is to exploit the mobility of Au nanodroplets at high temperatures. Fig. 7a shows the change in growth direction of some ZnO nanowires on GaN that repeatedly occurs upon encountering a physical barrier, in this case, another nanowire. The nanowire marked with a red arrow initially grows in a straight path until it reaches the nanowire denoted with a blue arrow. The effect is shown schematically in Fig. 7b. Once a ZnO nanowire approaches another nanowire, its native Au nanodroplet undergoes a two-stage migration. The first stage occurs when the droplet encounters the second nanowire,

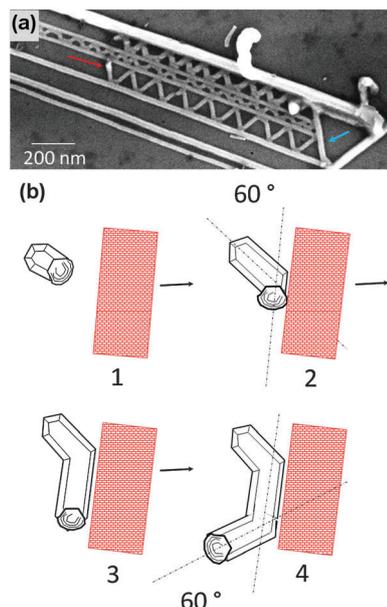


Fig. 7 (a) Change in the growth direction due to artificial barriers. This image also highlights the impact of hexagonal structure of the GaN substrate on the growth direction. (b) SEM data supports a sequence of events in which the Au droplet moves to a neighboring facet upon encountering an external surface. Each Au droplet migration results in a 60° rotation in the growth direction.

at which point it undergoes a change in direction of 60° . The second stage occurs when the nanowire reflects and changes direction by another 60° . This behaviour has two important implications. The first is that the Au droplet minimizes its interface energy with ZnO and prefers to interface with one facet at a time. The second is that by causing steric hindrance around some of the six facets of a ZnO island, one can limit the growth to specific facets. This concept is schematically shown in Fig. 8a in which nanowires are shown at their very early stage of growth, *i.e.*, as ZnO islands on a GaN substrate. Each island holds one Au droplet, which has been omitted in the graph for simplicity. By placing the islands along the $\pm[1\bar{1}00]$ direction of GaN, the facets that are normal to this direction are in close proximity of each other and their horizontal growth would be prohibited due to absence of the Au droplet on those facets. If the Au nanodroplets attached to the two neighbouring islands happen to be in close proximity to each other, they are most likely to combine, forming a larger nanodroplet and increasing the chance of forming a free standing nanowire. As a result of this treatment, the number of active growth directions is reduced from six down to four (small arrows in Fig. 8a). Furthermore, by choosing the direction of the carrier gas stream (blue arrow), it is also possible to suppress two more of the growth directions (red arrows, Fig. 8a). This is illustrated in the bi-directional assembly of ZnO nanowires on GaN shown in Fig. 8b. Therefore, having knowledge on crystallographic axes of the substrate and using the SVLS technique it is possible to control the number of growth directions in an assembly.

The growth of horizontal ZnO nanowires can also be controlled in the direction normal to the substrate for making 2D-nanostructures. This can be achieved by combining the SVLS and VS

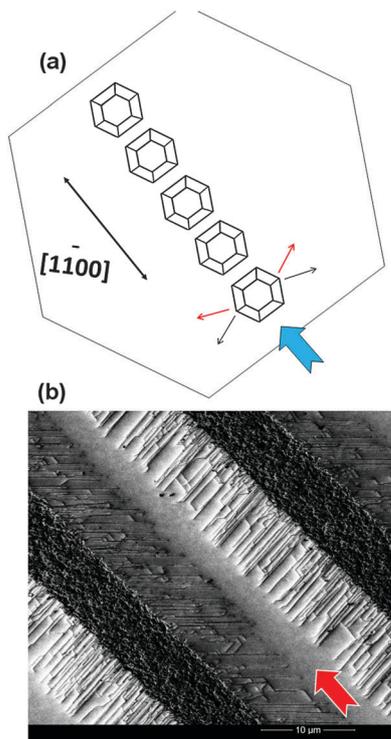


Fig. 8 Controlling the number of nanowire growth directions in an assembly of Au droplets. (a) An array of ZnO islands arranged in $[1\bar{1}00]$ direction of a GaN surface. Each island has six potential growth directions. Steric hindrance and gas flow direction can be used to reduce the number of growth directions from six to two. An example is shown in (b) where the nanowires assembly only shows two major growth directions.

growth processes. In this combination, as the nanowire grows on the substrate surface, the slow VS growth takes place on the (0002) facet of a nanowire, resulting in nanowalls with pristine surfaces, shown in Fig. 9a. As illustrated in Fig. 9b, nanowalls are typically about 80 nm to 100 nm in width and few microns in height. The VS growth starts as soon as a nanowire initiates its lateral growth on the surface. As such, their height is maximum at the initial growth site and minimal at the leading end of the nanowall. Nanowalls are commonly observed when an Au layer thicker than 20 nm is used as catalyst. It is possible that the Au clusters or atoms deposited on the ZnO (0002) plane act as promoters for the catalytic growth process in the $[0001]$ direction of the nanowire. This type of growth has also been observed in the formation of ZnO nanocantilevers and found to be due to the formation of Zn clusters on the (0002) polar surface of the ZnO nanowires.²⁷

The polar surface of ZnO nanowires is formed due to the asymmetric atomic structure of ZnO along its c -direction. The growth in this direction is faster, and as a result, the common growth direction of hexagonal structures like ZnO is $[0002]$ (the c -axis). Such structures are useful in piezoelectric applications, but are not desired for applications where high efficiency of radiative recombination of electron-hole pairs is critical. This is because the strain-induced piezoelectric fields reduce recombination *via* spatial separation of electrons and holes.^{102,103} As such, the growth of nonpolar substrates or facets have become of great interest for

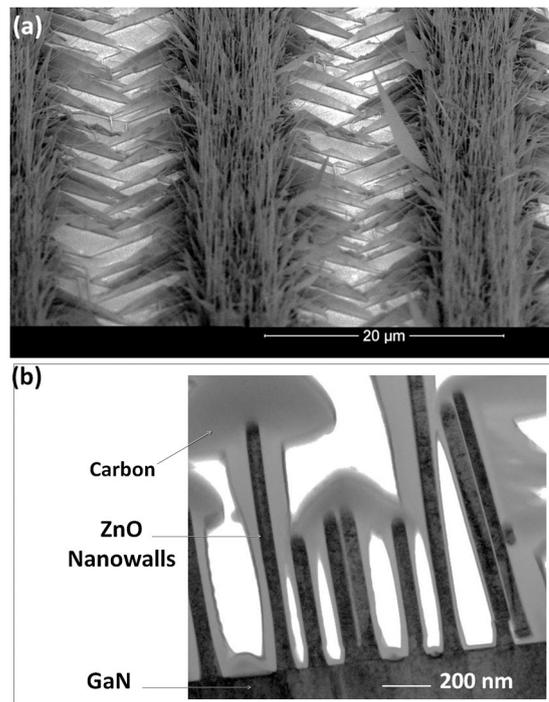


Fig. 9 An oblique view of arrays of ZnO nanowalls grown on GaN. Free-standing nanowires are also grown from Au droplets inside the patterns. (b) TEM cross-section of nanowalls shows the elongation of their second dimension along the ZnO polar direction; their narrow width distribution of nanowalls is also noticeable.

improving the efficiency of light emitting devices. Results show two types of side facets for ZnO nanowalls. In one group, they are confined to nonpolar a -planes ($11\bar{2}0$) that are upright in orientation (Fig. 9b); in another group, they are confined to semi-polar facets that are slightly inclined giving the nanowalls a triangular cross-section. Both groups of facets are flat originating from the semi-polar side walls of $(11\bar{2}2)$ shown in Fig. 5(b).⁹⁹ This is an important characteristic, as the smoothness and angle of the crystal facets are of great importance for the realization of low loss cavities or waveguides in electro-optical devices.¹⁰³ To make non-polar facets, there are conventional techniques, such as cleaving crystals and chemical etch; however, they become more challenging as facet size becomes small. Recently, to fabricate arrays of non-polar nanoscale facets of GaN, nanopatterning using electron-beam lithography was used to open nucleation sites on a masked sapphire substrate. GaN nanosheets were then grown epitaxially on the sapphire, which can be used for growth of quantum wells and other heterostructures.¹⁰² Laterally grown nanowalls could be of interest in 3D-architectures where the height of the nanoobjects is of significance; for instance, in applications where a higher surface area or a larger light absorption cross-section is desired. In the following sections some of these architectures are described with potential applications in light and energy generators and photocatalysis.

3.2.2 STRUCTURAL CHARACTERISTICS. Besides the structural quality of a nanowire, the realization of any higher device functionality, *e.g.*, a high speed or low power consumption will depend significantly on its boundary conditions and on the quality of nanowire interfaces with the rest of the device. This constraint applies to all

the nanowires active in a device; as such it is important to be able to reproduce similar interfaces as well as to control and predict the extent of their defects. In the *in situ* growth of horizontal nanowires using the SVLS method, since the interfaces of horizontal nanowires are formed simultaneously, their structures are expected to be quite similar. This is an important feature that could enable quality control of a massive number of nanowire devices such as p-n junctions, quantum wells, or transistors in a short period of time. In this section we will describe some of our results on the crystal quality of laterally grown nanowires and nanowalls and their interfaces with substrates such as sapphire and GaN.

Sapphire, due to its dielectric properties and high thermal conductivity, is a commonly used substrate for the growth of large band-gap semiconductors for light emitting devices and high power electronics. The lateral growth of ZnO nanowires on the *a*-plane of sapphire results in nanowires with a diameter ranging from 1 nm to 100 nm. As described previously, the diameter of nanowires is correlated with the size of the Au nanodroplets, and therefore can be reasonably controlled.⁸² Post-growth TEM analyses show that sapphire undergoes a substantial deformation at its interface with ZnO, which includes compressed and expanded regions. The sapphire crystal reconstructs, forming V-shaped interfaces with the nanowires in order to lower its lattice mismatch (Fig. 10a). ZnO, also experiences a strain, which is diameter dependant. As the diameter of the nanowire increases above about 25 nm, it partially or fully relaxes its strain, the V-shaped interface appears more flat, and ZnO facets become well-developed (Fig. 10b).⁹⁹ The side facet angle with the surface normal is about 32°, which is similar to the structure observed for ZnO nanowires on GaN (Fig. 5). In most studied cases, as the diameter of the nanowire decreases, a compressive strain develops along the [0001] direction, which reaches approximately 7% or less at the base of the nanowire. This is an indirect indication of the expansion of the nanowire at its base in order to minimize its lattice mismatch with the sapphire.

In contrast to sapphire, ZnO and GaN exhibit the same wurtzite crystal structure and have very similar lattice constants. GaN is a direct bandgap semiconductor and, with an electron-hole binding energy of about 24 meV is one of the widely used materials in light emitting diodes. ZnO, with a direct bandgap of about 3.3 eV, has attracted a lot of interest for UV light emission, lasing, piezoelectric devices,¹⁰⁴ transparent circuitry,¹⁰⁵ and photovoltaics.³⁰ Its band gap can be engineered by the addition of Mg or Cd dopants, which are inexpensive and abundant.¹⁰⁶ More importantly, ZnO exhibits one of the highest exciton binding energies (about 60 meV), which makes it a great material for high efficiency UV-visible light emitters compared to GaN. ZnO films have been typically grown by techniques such as chemical vapour deposition, pulsed laser deposition, sputtering, and molecular beam epitaxy.¹⁰⁷ In the case of epitaxial growth on GaN, a commonly observed characteristic has been the existence of large amount of defects or threading dislocations either extending from the GaN substrate or originated at the interface.¹⁰⁸ A similar behaviour is observed in homoepitaxial growth of GaN, and as such there is a great desire to develop growth methods with a reduced number of threading dislocations and

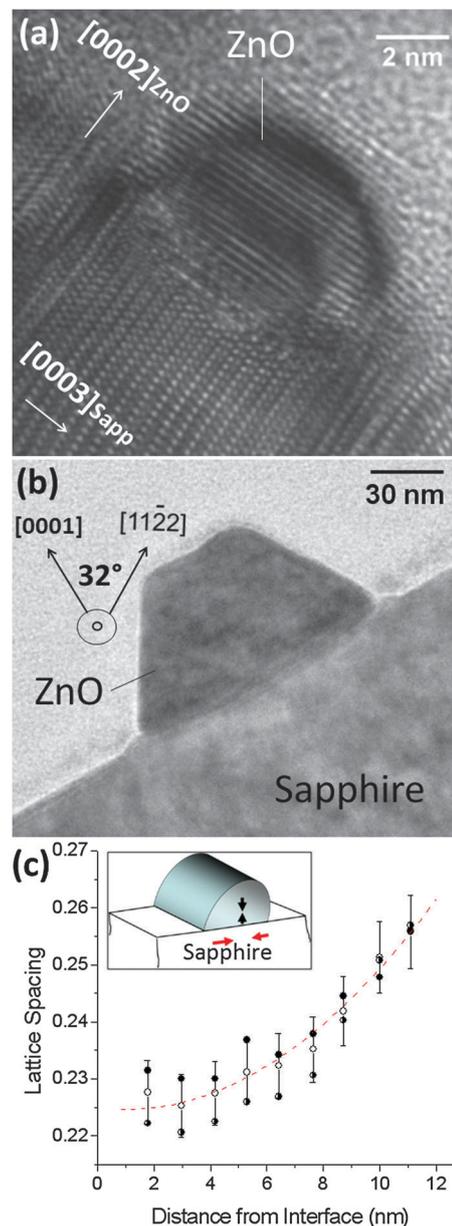


Fig. 10 Cross-sections of small and large size ZnO nanowires grown on *a*-plane sapphire. (a) Cross-section of a nanowire with ≈ 10 nm diameter shows the crystal orientation of the two crystals with respect to each other: *c*-plane of ZnO perpendicular to the *c*-plane of sapphire. Sapphire in its [0003] direction undergoes a considerable amount of strain to lower its mismatch with ZnO. Part of this strain leads to the reconstruction of sapphire around the nanowire creating a false perception that the ZnO has penetrated into the sapphire. (b) Large diameter ZnO nanowires show a more relaxed ZnO lattice with well-developed facets. The semi-polar side facet is tilted 32° from surface normal. (c) In ZnO, the lattice spacing decreases from top to its base at the interface indicating a lattice compression in the *c*-direction.

other defects that enhance the radiative recombination of charge carriers.¹⁰⁹ As discussed later, the SVLS growth of ZnO nanostructures on p-GaN produces formation of abrupt and high quality heterojunctions with no detectable threading dislocation⁹⁶ that offers new possibilities in integrating 1D- and 2D-ZnO nanostructures to the nitride family of semiconductors such as

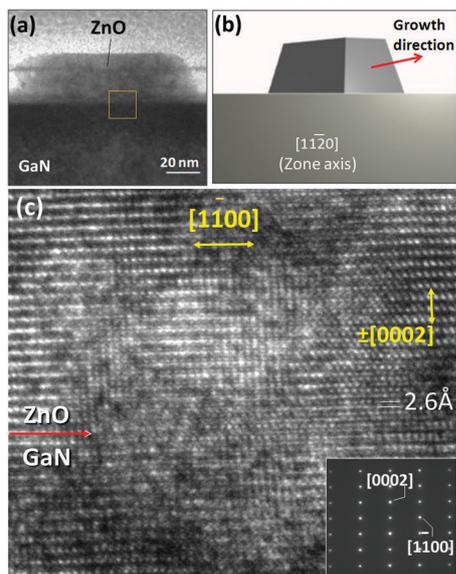


Fig. 11 (a) TEM image of a ZnO nanowire–GaN interface 30 degrees tilted relative to the optic axis. (b) This cross-section is viewed from $[11\bar{2}0]$ zone axis. (c) HRTEM image of the ZnO–GaN junction highlighted in part (a) and its SAED pattern in the inset. The heterojunction interface is shown with an arrow. The SAED pattern supports an epitaxial relationship between the two crystals.

GaN or InGaN for realization of multi-color light sources at large- or nanoscales.

Heterojunctions of ZnO nanowires and nanowalls with p- and n-GaN have been examined from three different perspectives: normal to the growth direction, tilted 30° from the growth direction, and top view. A representative cross-section of a ZnO nanowire on GaN is shown in Fig. 11a, accompanied by its schematic in Fig. 11b for a better illustration. After the specimen is tilted, the plane of view becomes (zone axis) $[11\bar{2}0]$ at which the ZnO plane spacing is larger, thus allowing for easier detection of interface defects. Examining the ZnO–GaN heterojunctions using HRTEM shows a fairly coherent relationship at the interface (Fig. 11c). The SAED pattern shown in the inset shows the *c*- and *m*-directions of the ZnO nanocrystal; it also indicates an epitaxial relationship between the two crystals and a single crystal structure. The top view cross-section of a laterally grown ZnO nanowire on GaN is shown in Fig. 12a in which part of a nanowire as well as the Au nanodroplet at its end can be seen. The low magnification image provides some information about the longer range quality of such nanowires and the lack of defects such as twin structures or a polycrystalline phase as the nanowire grows segment by segment (refer to Section 3.1.3). HRTEM of part of the nanowire in Fig. 12b shows the hexagonal order of atoms in the *c*-plane of ZnO and GaN. The inset diffraction pattern is consistent with the results obtained from side cross-sections indicating an absence of detectable defects. ZnO nanowalls were examined in the same manner. As described earlier, a nanowall is a result of the nanowire growth in its *c*-direction. Their structural analyses are similar to the nanowires. HRTEM examination of their interfaces indicate that the single crystal ZnO maintains the

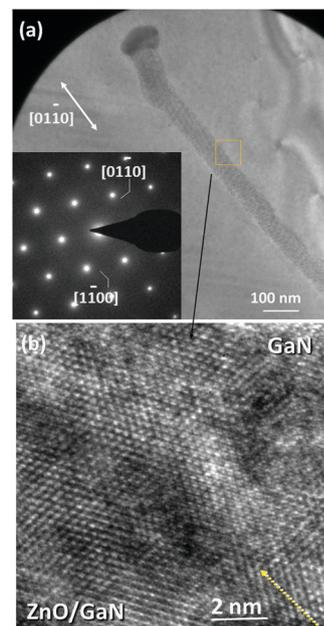


Fig. 12 (a) Top-view cross-section of a horizontally grown ZnO nanowire on GaN. SAED pattern from this perspective also confirms a single crystal structure. ZnO and GaN diffraction spots overlap with each other, because of the similarity of the two crystals. HRTEM image of the marked box interface shown in part (b) denotes only the hexagonal close-pack of atoms as well as a subtle contrast difference between the two sections.

orientation of the GaN substrate, namely, $(0002)_{\text{ZnO}} \parallel (0002)_{\text{GaN}}$ and $[\bar{1}100]_{\text{ZnO}} \parallel [\bar{1}100]_{\text{GaN}}$. Results also show nearly coherent and abrupt interfaces without formation of an amorphous GaO layer or any reaction layer despite the high growth temperature (900°C).⁹⁹

Cross-sectional analysis of nanowalls along their length can provide useful information such as how the defects propagate along the growth direction as new islands gradually form. Since this is a successive growth process, the crystal quality that is observed in one segment of a nanowire or nanowall is expected to be a representative of the ZnO–GaN heterojunction throughout the nanostructure. In most examined regions, ZnO exhibits a crystal structure with no detectable defects such as twin boundaries.¹¹⁰ Scattered stacking faults are observed that appear to be parallel to the interface (arrows in Fig. 13); such defects have been previously observed in free standing nanowires grown in their *c*-direction.¹¹¹ Observation shows that the stacking faults are local and do not propagate along the nanowires or nanowalls as new segments are added to the nanowire.

Furthermore, with respect to misfit dislocations at the interface, we observe a small number of them. In a fully relaxed ZnO thin film on GaN, the 1.8% lattice mismatch is expected to result in formation of misfit dislocations at every 15.8 nm (along $(\bar{1}100)$), which is not observed in the studied cross-sections.⁹⁹ This indicates a partial lattice relaxation that also agrees with the observed strain at the interface. Therefore in each 20 nm segment along the length of the nanowalls or nanowires, we estimate to have coherent regions with stored strain, and partially relaxed regions. We did not observe extension of defects such as threading

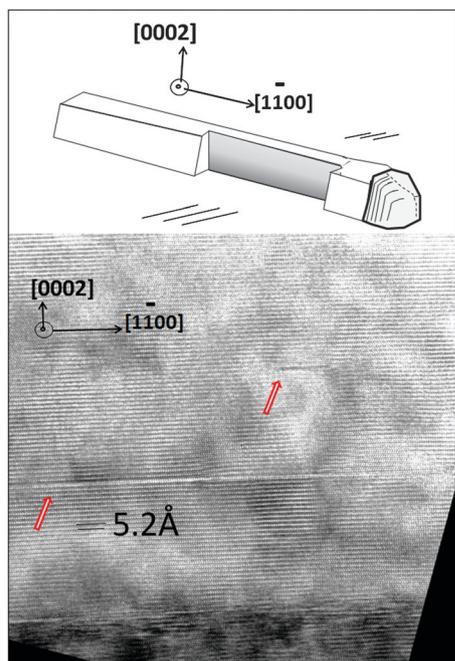


Fig. 13 (Top) Schematic of a nanowire cross-section along its length, which is shown at the bottom. In general, the examined cross-sections show a small variety of defects in the ZnO region. The HRTEM image shows two stacking faults (red arrows) in the ZnO region that do not fully glide through the crystal. Two crystallographic directions are shown in both graphs to better portray the position of the interface. The darker part of the image represents the GaN side.

dislocations to the ZnO phase, which is a distinct advantage of one-dimensional ZnO–GaN heterojunctions. This type of defect is notorious in creating non-radiative recombination centers and reducing the performance of light generation in electro-optical devices such as LEDs.¹⁰⁹ Overall, in comparison with the thin ZnO films grown at the interface between free standing ZnO nanowires and GaN, the results herein show that the SVLS method leads to significantly lower structural defects.¹¹²

3.3 Growth modes of vertically aligned nanowires

Growing vertically aligned nanowires has shown great promise for designing and fabricating novel nanowire-based electrical, optical, and piezoelectric devices.^{113–115} Such devices would potentially offer higher performance compared to conventional 2D thin film devices. As discussed in earlier sections, the aligned morphology can be controlled by the epitaxial relationship with the single-crystal substrate¹¹⁶ or the deposited nanocrystal seeds on the substrate.¹¹⁷ In most cases, the supporting substrates are different materials from the nanowires due to factors such as substrate availability or the demands of the application. For example, ZnO nanowire arrays have been grown on GaN, AlN, SiC, Si, and sapphire substrates.¹¹⁸ Vertical alignment of ZnO nanowires was first demonstrated on *a*-plane orientated sapphire substrates.¹¹⁵ In this technique, growth is initiated and guided by Au nanoparticle catalysts and the epitaxial relationship between ZnO and sapphire leads to the alignment. In 2004, Wang *et al.* combined a self-assembly masking technique with surface epitaxial confinement to

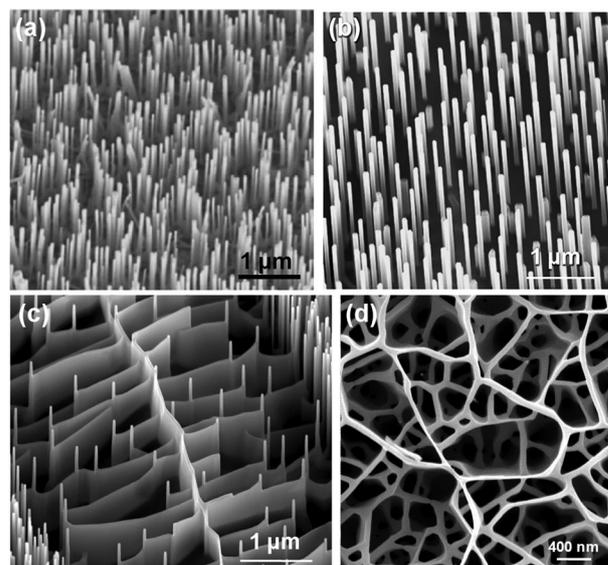


Fig. 14 (a) Vertically aligned and hexagonally patterned ZnO nanowires grown on sapphire substrate. (b) Randomly distributed aligned ZnO nanowires grown *via* VS process. (c) Parallel ZnO nanofin structures. (d) Randomly distributed ZnO nanowall networks.

grow vertically aligned ZnO nanowires with hexagonal patterns in large areas (Fig. 14a).¹¹³ In this approach, a monolayer of close-packed polystyrene nanospheres was self-assembled on a sapphire substrate, acting as a shadow mask for Au catalyst deposition. After the nanospheres were etched away, hexagonal Au patterns were left on the substrate, from which hexagonal arrays of ZnO nanowires were grown *via* the VLS process.

VS growth process can be utilized in aligned growth of ZnO nanowires without introducing metal catalyst nanoparticles. It is believed that this process is preceded by the random precipitation of Zn clusters from the vapour phase, and thus no control over the distribution of nanowires is possible in this case (Fig. 14b). When the temperature is sufficiently high, the Zn cluster can move laterally across the substrate during the ZnO deposition. As such, ZnO is deposited along the drifting path and the nanowire morphology is converted to vertical ZnO nanofin arrays.¹¹⁹ Similar to nanowalls described in the previous section, the nanofin structure can be as tall as the nanowire (several micrometers) with a thickness of only tens of nanometres. Typically, termination of the nanofin occurs when it reaches a junction with the side wall of a nanowire, where the two structures merge. The spatial distribution of the ZnO nanofins can be controlled by designing a surface feature that would define the drifting path of the Zn clusters. By first depositing a “hill” shaped ZnO epitaxial base layer, most Zn clusters are nucleated along the central line at the summit of the “hill”. Following the inclined base surface, Zn clusters drift to the bottom of the “hill” and initiate the formation of ZnO nanofins that are approximately parallel to each other, as shown in Fig. 14c. Due to the existence of a central wall, which possibly results from the dense nucleation sites along the summit, the vertical nanofins exhibit a more uniform height from their original positions to their termination where it reaches another nanowire. When the

substrate is flat, drifting of Zn clusters becomes completely random and is controlled by Brownian motion. A high density of the Zn clusters would also make nanofins quickly intersect with each other, terminating the growth process and resulting in a network (Fig. 14d) that can be considered as traces of the drifted Zn clusters. Due to intersection, the drifting stops quickly and the Zn clusters start to grow into vertical ZnO nanowires. Because of the higher vapour concentration and the small distance between ZnO nanowires, the space between them could be quickly filled by a thin wall of ZnO. Therefore, led by the growth of nanowires, a continuous nanowall network could be formed (Fig. 14d). Since the nanowall locations follows the Brownian motion traces of the mobile Zn clusters, their distribution should not follow the substrate lattice.

A wide range of nanowire–substrate combinations have been generated capable of producing free standing nanowire arrays. Germanium, silicon and InAs nanowires have been grown on Si substrates.^{120,121} GaAs and InGaAs have both been reported as substrates for InAs nanowire arrays.¹²² GaN nanowire arrays have been grown on SiC.¹²³ This list is by no means exhaustive, but gives a general feel for the versatility of the technique across a large grouping of materials.

While the range of material combinations that have been demonstrated to be capable of yielding vertical nanowire arrays is impressive, a thorough understanding of how to grow uniform, well-controlled, and perfectly aligned nanowire arrays has not yet been achieved. For example, the size of nanowires is typically defined by the size of metal catalyst nanoparticles used; however, the small lattice mismatch between the nanowires and the substrate is believed to make a significant contribution to the final nanowire morphology. In this regard, the lattice mismatching effect was recently investigated by adapting the Stranski–Krastanow (SK) thin film growth model to understanding the epitaxial growth phenomena of nanowires on heterogeneous substrates.¹²⁴

For nanowires grown epitaxially on heterogeneous substrates, three growth behaviours have been identified. First, nanowires can grow vertically on a thin film of the same material formed on the

surface of the substrate (Fig. 15a). This film serves as a buffer layer and nanowires grown from it should thus be considered as having undergone homo-epitaxial growth. The high density of nucleation sites due to dense catalyst coverage and high vapour concentration of the source gas is believed to be the main reason for the formation of this film. Fig. 15d shows such a situation where vertical ZnO nanowires grew on a very thin layer of a ZnO network. The size of these nanowires exhibits a wide distribution, due to the lack of uniformity in the nucleation sites. In addition, the Au catalyst droplets can be clearly seen on top of these nanowires, indicating that they were formed *via* a VLS process. Most vertically aligned ZnO nanowires synthesized by vapour deposition belong to this mode, where a thick defective ZnO thin film is always present beneath the vertically oriented, strain-free ZnO nanowires.¹¹² Due to the appearance of a defective heteroepitaxial thin film (or continuous network) prior to the nanowire formation, this growth behaviour is attributed to the general SK mode.

Under other conditions, a large, cone-shaped base would form beneath a long, vertical ZnO nanowire with a uniform diameter (Fig. 15b). Experimental observations show that the diameter of nanowires grown in this mode is smaller and the size distribution narrower than those grown in the SK mode. This mode is commonly observed when vertically aligned nanowires are grown discretely (Fig. 15e). Similar to the case of the continuous film, the large base beneath the nanowire may also contain dislocations in order to reduce the misfit strain energy at the interface. Therefore, this behaviour is simply a modified SK mode, and is normally referred to as the island SK (i-SK) mode.

The least observed growth phenomenon occurs when vertical nanowires grow on a bare substrate surface without any transition structures (Fig. 15c). Fig. 15f shows that these types of nanowires exhibit the smallest average size and the narrowest size distribution. Nanowires with such small sizes were generally discovered to be dislocation free, and, accordingly, this growth behaviour is defined as the coherent SK (c-SK) mode. The SK, i-SK and c-SK modes cover all the observed growth phenomena when vertical nanowires are grown epitaxially on heterogeneous substrates. Among them, the c-SK mode is the most desired due to the uniform dimension of each resulting nanowire and the overall nanowire size distribution.

These three growth modes can be defined by a strain *versus* dislocation (SVD) model, which describes the competition between the strain energy and the dislocation energy at the interface between the nanowire and the substrate. The nanowire length where these two energies become equal is defined as the critical length (H^*). Ideally, dislocation-free nanowires with a given radius could only be formed with a length smaller than H^* . Calculating H^* at different radii generated a series of points that defined the H^* *versus* R relationship, which is shown by the solid diamond markers in Fig. 16. The critical length quickly increases from a few nanometers to infinity, where the nanowire radius is defined as the critical radius. The H^* – R curve can be used to predict the growth behaviour and nanowire dimensions. Lengths and radii were measured from ZnO nanowires synthesized from various experimental batches and plotted together with the curve to show how the three growth modes are related to the H^* – R curve. All the

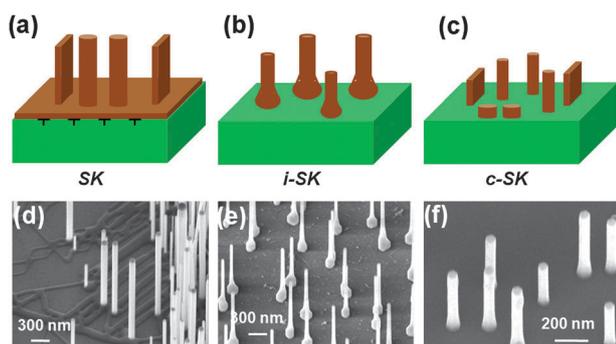


Fig. 15 Three suggested heteroepitaxial growth modes of nanowires. (a) The SK mode, where a defective film forms between the solid substrate and strain-free nanowires. (b) The island SK (i-SK) mode, where a cone-shaped base forms beneath the nanowire. (c) The coherent SK (c-SK) mode, where dislocation-free nanowires directly grows on the substrate surface without any intermediate structure. (d–f) Typical SEM images showing ZnO nanowires grown on GaN substrate *via* the SK, i-SK, and c-SK modes, respectively.

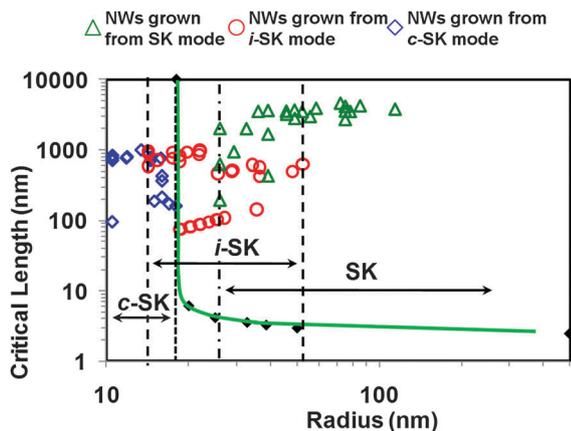


Fig. 16 Critical length versus radius plot of dislocation free ZnO nanowires. Triangle, circle, and diamond markers are experimental data measured from ZnO nanowires grown on GaN substrate via SK, i-SK, and c-SK modes, respectively.

c-SK-grown nanowires (star markers) lie on the left-hand-side of the curve. This demonstrates that the SVD model is able to predict the critical diameter of dislocation-free nanowires that can be vertically and uniformly grown on heterogeneous substrates.

The i-SK grown nanowires are marked as circles in the plot. They exhibited larger diameters and are distributed on both sides of the H^*-R curve. The increasing trend of the nanowire diameter indicates that the base formed under such nanowires was capable of releasing the interfacial strain energy, thus providing a nearly strain-free, homoepitaxial growth platform. For the nanowires grown via the SK mode, both their diameter and distribution were larger than those measured from the c-SK and i-SK modes. This observation strongly supported the statement that the underlying defective ZnO film accommodated all the compressive strain, and thus nanowires could grow with an “unlimited” length and width. In reality, under these circumstances, the size of nanowires is controlled by the catalyst particles or the fundamental thermodynamic parameters. The relationship between the growth modes and the H^*-R curve clearly show that the SVD model is properly established and could serve as an effective guidance for designing vertically aligned nanowires on heterogeneous substrates.

3.3.1 GROWTH OF 3D NANOWIRE ARRAYS. 3D nanowire arrays represent a promising architecture that features an extremely large surface area as well as tuneable electronic properties. These advantages make 3D nanowire architecture exceptionally advantageous for many energy-related systems, whose performance is dependent on surface reactions and bulk charge transportation: including third-generation photovoltaic devices, photoelectrochemical (PEC) catalysts, hydrogen storage systems, and battery electrodes.¹²⁵ The unique merits of 3D nanowire architectures are well recognized in a number of scientific disciplines, and intensive research efforts have been devoted to the fabrication of such structures and the control of their properties. Representative bottom-up synthesis strategies include direct growth of nanowire networks and the sequential growth of nanowire branches. The direct growth of 3D nanowire architectures via vapour deposition integrates the formation of nanowire backbones and branches into one step, wherein the growth of nanowire branches is initiated by metal clusters that are precipitated simultaneously with

the backbone growth. The metal clusters can consist of the same element as the metallic component in the binary nanowire compound (*i.e.* Zn in a ZnO system) or a different material that is added to the growth atmosphere. For example, six-fold branched ZnO nanowires forming on the six equivalent side surface can be made by adding Sn to the ZnO precursor.¹²⁶ Similarly, bundles of orthogonally branched PbSe 3D nanowire networks were grown by introducing In or Ga as the secondary nucleation seeds.¹²⁷ However, self-catalyzed branching growth is a more commonly reported case. When condensation of the metal component is not immediately compensated by the combination of compound formation, branched growth would occur. This phenomenon is more prominent for compounds where the metal component has a high vapour pressure or the compound formation enthalpy is high. For example, lead chalcogenide, metal silicide, and tungsten oxide usually exhibit such branched growth behaviour.^{128–132} Nevertheless, this strategy only applies to the synthesis of 3D homogeneous nanowire networks under well controlled conditions. Compared to the direct growth of 3D nanowire networks, the sequential growth of nanowire branches exhibits better versatility in selecting different materials and forming heterojunctions, which is essential for realizing many applications that utilize their semiconductor properties. This synthesis strategy typically requires an additional step of applying seeds on the central nanowire backbones after they are formed.^{133,134}

Although these 3D nanowire networks exhibit tuneable electronic properties, the surface area density is still considerably smaller than what can be achieved using 3D nanoparticle networks. Intuitively, a desired improvement would be to increase the volume density of the nanowire branches, resulting in a decrease of the spaces between individual nanowires down to at least the hundreds nanometer regime. Unfortunately, when the spacing scales down from micrometer to sub-micrometer, the growth of nanowire becomes seriously impaired. This is due to the coupling between crystal growth and precursor concentration that is often dictated by the mass flow characteristic of vapour or liquid phase reactants within the highly-confined spaces between nanowires. Recently, Shi *et al.* developed a surface-reaction-limited pulsed chemical vapour deposition (SPCVD) technique that effectively decoupled the nanowire growth from vapour concentration.¹³⁵ Through this technique, single-crystalline anatase TiO₂ nanowires were uniformly grown covering the entire inner surface of highly-confined anodic aluminium oxide (AAO) nanochannels. The resulting TiO₂ nanowire coated AAO channel is shown in Fig. 17. Fig. 17a shows the cross section of the 53 μm -long AAO channels after 660 cycles of SPCVD growth. SEM images acquired from the top, middle and bottom sections are shown in Fig. 17(b–d), respectively, revealing the uniform and dense coverage of TiO₂ nanowires along the entire channel length. Closer examination shows that all nanowires were rooted on the walls of the AAO channels and pointed inward (Fig. 17e). The majority of the as-synthesized TiO₂ nanowires had lengths and widths of between 170 nm–210 nm and 25 nm–30 nm, respectively. TEM and XRD spectra revealed that the nanowires were single-crystalline anatase TiO₂. As shown in Fig. 18, Shi *et al.* also demonstrated a uniform coverage of TiO₂ nanowires on the entire surface of dense Si nanowires.¹³⁶ The Si nanowires used in the experiments were

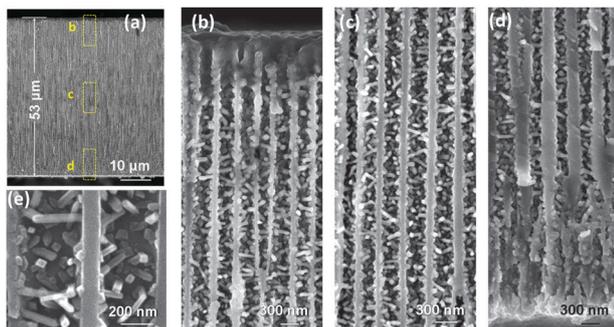


Fig. 17 TiO_2 nanowires grown in nanochannels. (a) Overview of a cross section of the AAO template after 660 growth cycles. (b–d) Higher magnification SEM images showing the uniform and dense coating of TiO_2 nanowires within the AAO channels at the top, middle, and bottom sections, respectively, as indicated by the dashed yellow boxes in (a). (e) TiO_2 nanowires rooted on the walls of AAO channels showing a squarelike cross section and well-faceted shape.

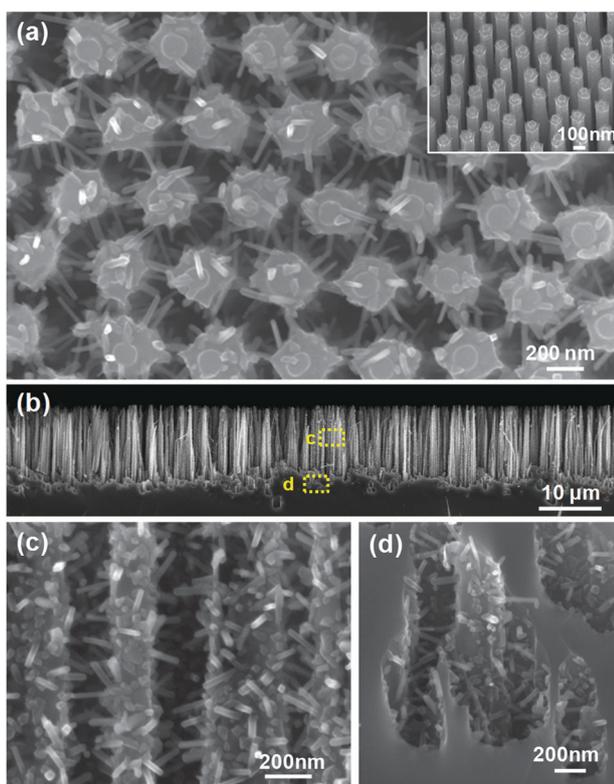


Fig. 18 Si nanowire arrays uniformly covered with high-density TiO_2 nanowires that grew laterally out of the side surfaces. Inset shows the cross-section of TiO_2 nanowire-coated Si nanowire arrays.

fabricated by deep reactive ion etching (RIE) using silica spheres as a mask. The lengths of the Si nanowires were $\sim 15 \mu\text{m}$ and the spaces in between were 200 nm–300 nm in width. This result demonstrated the versatility of the SPCVD technique for making TiO_2 nanowire arrays inside different material matrices.

The SPCVD technique utilizes separated precursor pulses (TiCl_4 and H_2O for the growth of TiO_2 nanowires) at a relatively high deposition temperature (600°C). This technique is essentially a successful conversion to anisotropic nanowire growth of

the atomic layer deposition (ALD) technique often used for conformal thin-film growth.¹³⁷ TEM observations and controlled experiments suggested that the formation of nanowire morphology is possibly due to the combined effect of two mechanisms: surface recombination and HCl restructuring. When the temperature is sufficiently high, the surface active species, such as Ti–OH groups, can react among themselves to form inactive Ti–O–Ti bonds in a surface recombination process. Different crystal surfaces would exhibit different reaction rates or activation energies for this recombination reaction, which may lead to the anisotropic growth rate and thus nanowire formation. On the other hand, HCl, a by-product of the deposition reaction, can also react with Ti–O–Ti groups and form Ti–OH and Ti–Cl surface groups. This can be considered as a reactivation process, where the rate is also surface-dependent. These two mechanisms do not conflict with each other and can proceed simultaneously. The combination of these two reactions will cause the active groups to move along the crystal surfaces and reach more stable sites where the recombination rate is low. Therefore, all the TiO_2 nanowires were observed to have grown along either the [002] or [011] directions. It would be possible to apply this mechanism to other functional materials that possess similar precursor and surface properties.

4. Challenges in scalable nanodevice integration

4.1. Nanowire-based light emitting devices

Irrespective of the nanodevice size, scaling up device integration requires parallel and high throughput interfacing. In this section, we discuss various designs for charge injection into 1D p–n heterojunctions. Applications are diverse including memory devices, logic circuits, sensory applications, light emitting devices and photovoltaics. In the earlier sections, we described some approaches for controlling the surface registries and orientation of nanocrystals on a given surface. These are some of the prerequisites for device integration if the goal is developing commercially viable technologies. A common goal in integrating nanocrystals to devices is to inject charge carriers to some specific sites. Different strategies have been utilized for integration of nanowire devices. In free-standing nanowire devices, heterojunctions are fabricated at the nanowire interface with the substrate where the charge recombination takes place.^{138–140} The typical poor quality of this interface can substantially deteriorate the performance of the light emitting device such as its lifetime, operating voltage and emitted wavelengths. In such platforms, the top contact can be placed on nanowires by depositing a conductive contact with a suitable work function to ensure a reasonable ohmic contact. For densely packed standing nanowires, the placement of the top contact requires simple deposition of an inorganic layer.¹⁴¹ For nanowires with a lower packing density, the voids are filled with different non-conducting materials including spin-on-glass,¹⁴² or polymers to further stabilize the nanowires.¹⁴³ One of the limitations of this design is the presence of highly defective ZnO thin film that forms at the interface, despite the

typical high quality of the rest of the nanowires.¹¹² In radial heterojunction designs, the active part of the device is the heterojunction between the ZnO nanowires and the counter electrode. The surface area of the heterojunction is a determining factor in the extent of charge recombination or separation in a device and depends on the fabrication process. As an example, in hybrid organic semiconductor-ZnO devices, the p-type polymers can be interfaced with only the top end of the n-type nanowires,¹⁴⁴ which results in an overall smaller heterojunction surface area; or it could be interfaced nearly with their entire length by deeper injection of the conductive polymer into the voids between nanowires.^{145,146} n-p homo-junctions of ZnO nanowire have been made axially within the free-standing nanowires. By placing a conductive layer on top and bottom of nanowires their light emission has been demonstrated.¹⁴⁷ Challenges in realization of ZnO homojunctions remains to be the difficulty in growing the p-type ZnO layers, and controlling their doping profile with high spatial resolution.^{148,149} In general, despite high quality of produced ZnO nanowire, their light emitting devices show some common weaknesses such as diversity in their emitted wavelengths and high operating voltages implicating deficiencies in the atomic structure of the device interfaces that must be addressed before realization of their optimal performance.

In planar integration of nanowires, the parallel interfacing is not as straightforward as that for the free standing nanowires. This is because the nanowires must be transferred to a target substrate for device fabrication, which requires performing nanowire alignment steps as described in Section 2. The intrinsic limitation of such alignment techniques is the lack of knowledge on the exact location of the active part of a device, *e.g.*, a heterojunction, quantum well or quantum dot. On a small scale, use of single- or multiple nanowire devices (in planar format) have been demonstrated for application such as solar cells,¹⁵⁰ and LEDs.¹⁵¹ On a larger scale, serial interfacing of nanowires containing heterojunctions is a slow process and not currently suitable for scaling up as it typically requires a high resolution technique for patterning.¹⁵² Pattern transfer techniques have become popular in large scale manipulation of micro- and nano-objects because of their capabilities in parallel interfacing.^{12,153} These techniques typically require a source substrate that contains the nanostructures, a pattern transfer mean and a target substrate. The minimum size of the formed nanostructures on the target substrate generally depends on the critical dimension of the patterns used in the printing process. As the pattern resolution increases, *i.e.*, toward single nanowire devices, its implementation and nanodevice fabrication becomes more challenging. On a commercial level, these techniques are expected to have a niche in applications where the active elements of the device are groups of nanowires, rather than individual ones. The growing need continues for developing methods with sufficient precisions in positioning and alignment of nanowires down to a single particle level.

The SVLS growth process is expected to have the potential to provide a high precision in determining the registry of the active segment of a device both at single or multiple particle

level. In general, the two basic requirements of this process are the deposition of metal catalyst patterns and an appropriate single crystal substrate to guide the growth. In realizing single particle devices on a large scale, the present limiting factor is the need for producing sub-50 nm single particles of the metal catalyst. Given the rapid growth in availability of high resolution micro-fabrication tools with affordable costs, this limitation is expected to fade away in the near future. Having said that the SVLS technique readily produces 10–20 nanowires per site using typical photolithography tools with a 1 μm resolution.⁸⁰ In the following, we discuss our recent progress on preparing large arrays of 1D- and 2D-ZnO nanostructure-based light emitting devices on GaN. ZnO has attracted a great deal of interest for UV light emission, lasing, piezoelectric devices,¹⁰⁴ “invisible” circuitry,¹⁰⁵ and photovoltaics.³⁰ Its band gap can also be engineered by the addition of Mg or Cd dopants, which are inexpensive and abundant.¹⁰⁶

Two simple charge injection designs are discussed that both highlight the ability of the SVLS growth process in parallel nanostructure interfacing. In one charge injection scheme as illustrated schematically in Fig. 19a, using the Ti/Au metal contact (yellow bar) electrons are injected to the ZnO backbone and then to the nanowalls, while holes are injected to the underlying p-type GaN substrate using a Ni/Au metal contact. Note that the ZnO backbone is the underlying continuous ZnO film that is formed during the formation of densely packed free-standing nanowires.¹¹² This film forms where the original Au pattern was deposited and possesses approximately the same dimensions. The relative location of nanowall arrays are known with respect to the global marks (not shown here), thus metal contacts can be readily deposited *via* standard photolithography techniques over the ZnO strips. Representative images of a three-layer (metal/ZnO nanowalls/GaN) structure are shown in Fig. 19(b–c), where the top metal electrode is deposited on the ZnO backbone. The overall shape and size of the nanowire LEDs can be tailored by the original Au pattern,

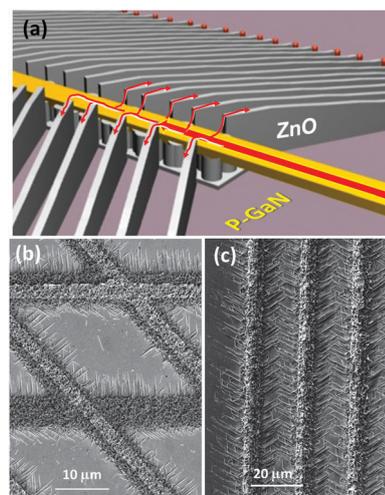


Fig. 19 (a) Schematic of the 1st design for charge injection to ZnO nanowalls *via* a ZnO backbone. As seen in (b–c), the top metal contacts are directly placed on the ZnO backbone.

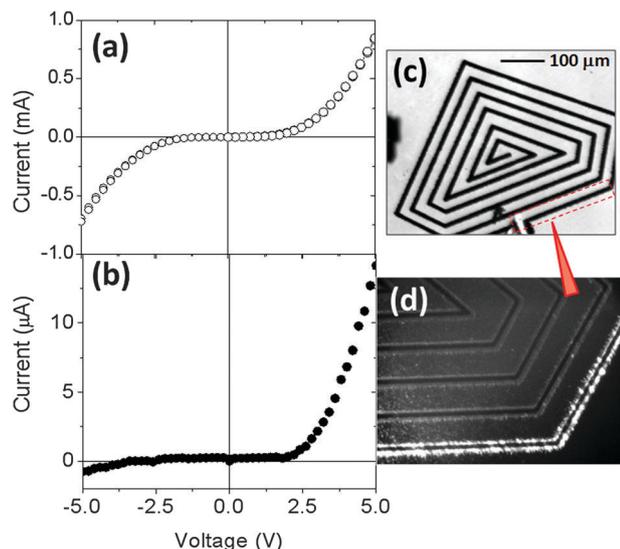


Fig. 20 (a) I - V scan of arrays of n - p heterojunctions of ZnO nanowalls on GaN. The overall device size is $5\text{ mm} \times 5\text{ mm}$. (b) I - V scan of a small array of n - p heterojunctions of ZnO nanowalls on GaN. The overall device length is $100\text{ }\mu\text{m}$. (c) Optical image of a 3.6 mm -long array of n - p heterojunctions of ZnO nanowalls on GaN. Nanowalls are grown off of the ZnO backbone, but cannot be resolved in this image. (d) Optical image of this device under forward bias shows that only part of the long array emits light.

which offers a unique platform for making microscale light sources.⁹⁶

Fig. 20(a and b), respectively, show the I - V scans of arrays of n - p heterojunctions of ZnO nanowalls on GaN in two large ($5\text{ mm} \times 5\text{ mm}$) and small ($100\text{ }\mu\text{m}$ wide) size devices. The doping level in the GaN layer is about $5 \times 10^{17}\text{ cm}^{-3}$ and the carrier concentration in ZnO is about $1 \times 10^{18}\text{ cm}^{-3}$ based on our previous results.⁸⁰ Both devices exhibit rectifying behaviors; it is also noted that in the larger device (Fig. 20b) the amount of transported current through the device at a given bias is higher, which is indicative of a larger number of nanowalls as conductive channels. The examined devices exhibit turn on voltages ranging from $2.7\text{ V} \pm 0.2\text{ V}$ to $3.8\text{ V} \pm 0.2\text{ V}$, and breakdown voltages of $3\text{ V} \pm 0.2\text{ V}$ to $9\text{ V} \pm 0.2\text{ V}$. Larger devices also show a lower breakdown voltage, which is mainly attributed to the existence of mid-bandgap states due to the formation of defects at the interface of the ZnO backbone and GaN. As the length of the ZnO backbone is reduced, *e.g.*, in smaller devices, the leakage at the reverse bias is reduced (Fig. 20b).⁹⁶ Fig. 20c shows an optical image of a single array device containing a five millimetre-long ZnO backbone with a polygon shape. This dark pattern is decorated with horizontal nanowalls which are not detectable in this image. Under an injection current of $\approx 0.9\text{ mA}$ at $+7\text{ V}$, the heterojunctions emit light as seen from the electroluminescence (EL) image in Fig. 20d. Since ZnO is in full contact with GaN, the e - h recombination sites are expected to be along the length of the heterojunctions, which also agrees with the observed emission along both nanowires and nanowalls in the EL images.⁹⁶ In mechanically formed p - n junctions emission originates from the sites where a nanowire contacts the substrate.^{151,152} One of

the drawbacks of this design is that the injected charges must go through the ZnO strip before reaching the nanowalls. A significant portion of the injected electrons are lost in the ZnO strip mainly due to non-radiative recombination at its interface with GaN. The drop in the injected electrons is such that only the first loop of this device is lit as seen in EL image of Fig. 20d. In addition, the ZnO strip has a certain resistivity that results in heating of the device during operation and thus a lower brightness, as well as potential structural damage.

An alternative charge injection design is shown in Fig. 21a. In this case, in order to reduce the loss of injected electrons, the top metal contact is directly placed on ZnO nanowalls but without connection to the GaN substrate. In doing so, the electrons are directly transported to the nanowalls and recombine with holes at their intersection with GaN. A representative cross-section of the fabricated devices and its schematic in Fig. 21a shows that a thin dielectric layer such as silicon oxide must be deposited on GaN prior to the placement of the top lead to avoid any short circuit. It is noted that the deposition of the dielectric layer must be unidirectional to ensure the sides of

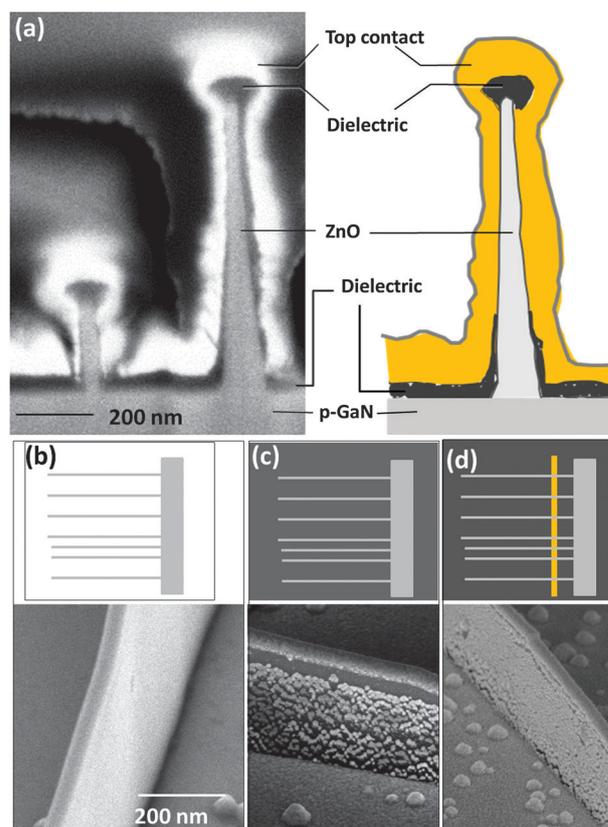


Fig. 21 An alternative charge injection design in which nanowalls are directly pumped with electrons. (a) SEM cross-section of two neighboring nanowalls with the corresponding schematic depicting all the device layers. (b) As grown ZnO nanowalls. (c) ZnO nanowalls after overcoating with about 50 nm of silicon oxide; as seen from SEM image, the ZnO side walls are still exposed. (d) Selective deposition of top contact on nanowalls using photolithography. After top contact deposition on nanowalls, the exposed areas of the ZnO side walls are fully coated with metal without any direct electrical contact with the underlying GaN surface.

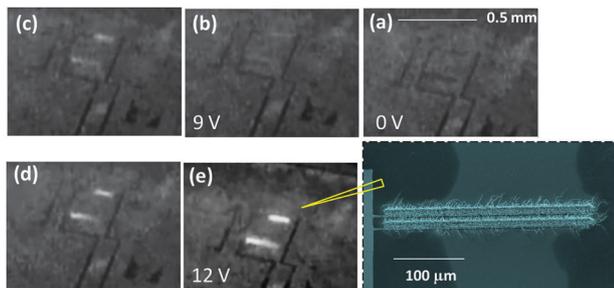


Fig. 22 A series of optical images of two parallel devices, which are about 300 μm distant and have a length of about 300 μm . The darker patterns in the images represent the top metal contacts. (a–e) as the forward bias increases from 0 to 12 V, the brightness of the emitting devices increases. Inset of figure (e) is a representative SEM image of heterojunction arrays of ZnO nanowalls on GaN.

the nanowalls remain uncoated or partially coated. This layer can be seen in Fig. 21a as the dark gray layer above the GaN surface. The sides of the nanowalls before and after silicon oxide deposition are shown in Fig. 21(b–d). By deposition of 125 nm of Ti/Au (15 nm/110 nm) as the top metal contact, the discontinuous oxide-coated side walls are fully coated (Fig. 21a). As shown in Fig. 21d (top), the top contact is deposited photolithographically directly on the nanowalls. Deposition must be performed at two tilt angles to ensure full coverage of nanowall sides with Ti/Au. This is the white layer seen in Fig. 21a, which is viewed from a tilted angle in Fig. 21d. One of the interesting aspects of this design is that the top metal electrode is connected to the non-polar facets of the ZnO in contrast to other designs where the polar facet of the nanowire is in contact. Another distinction is the use of a lower bias voltage for observing the light emission in the second design. Fig. 22(a–e) shows a series of optical images acquired from two sets of devices under a forward bias voltage ranging from 0 V to 12 V. The inset shows a SEM image of one of the devices, which includes two ZnO nanowall arrays, each about 300 μm in length and lateral spacing.

The emitted light from heterojunctions can be guided to a spectrometer for characterizing their spectral information. Using both device designs, the EL spectra of a number of heterojunction arrays with different shapes and sizes were studied at different forward and reverse bias voltages from -25 V to 27 V. At forward bias, the common characteristic is a strong excitonic emission at about 390 nm as seen in Fig. 23(a–b) (blue curves). The energy of this emission agrees well with the photoluminescence (PL) of ZnO nanowalls at 380 nm indicating that the recombination of the injected electrons and holes occurs within the ZnO side of the device. This is also in agreement with the observation that light was only emitted from the nanowalls and not from the surrounding GaN substrate (Fig. 20d and 22e). The strong excitonic emission and the absence of deep trap emissions at about 550 nm are both indicative of a low density of traps and defects at the interface. The second design requires a lower bias to operate in comparison with the first design. Furthermore, the breakdown voltage and leakage of the device is substantially reduced as a result of minimizing the contribution of the ZnO backbone in the charge injection process.

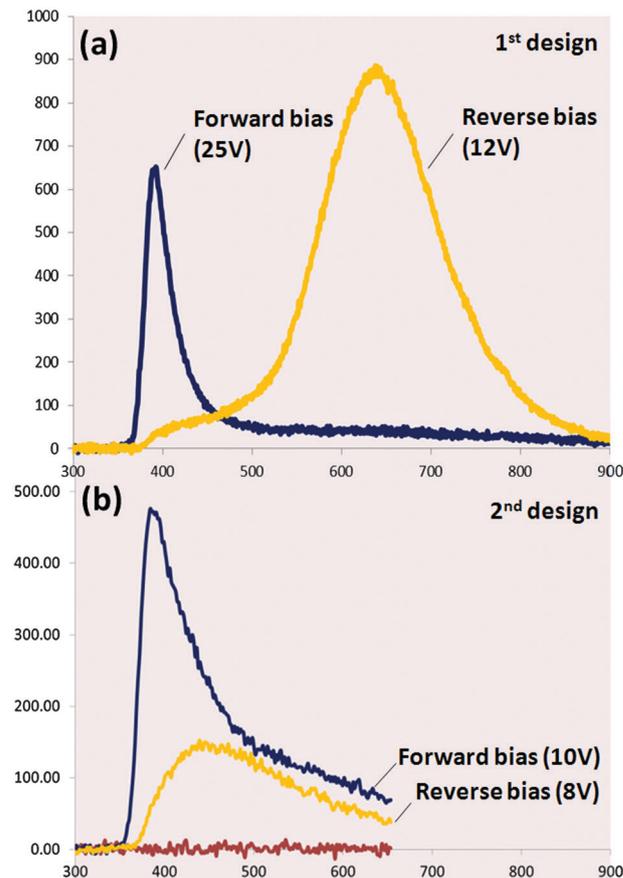


Fig. 23 Comparison of the electroluminescence spectra of the two charge injection designs. (a) First design: a 400 nm emission (blue curve) at forward bias is observed, which resembles that of the second charge injection design as shown in graph (b, blue curve). The clear distinction between the two designs is the presence of the 640 nm emission in graph (a) and its absence in the second design (graph b).

An example of a sizeable charge transport through the device at the reverse bias voltage is shown in Fig. 20a. At this bias, typically above 6 V, the device emits a bright orange emission centered at about 640 nm (Fig. 23a, yellow curve). This emission is absent in the second diode design (Fig. 23b, yellow curve). This emission is not observed in the PL of the corresponding ZnO arrays on GaN; however, it has been observed in oxygen-rich ZnO films obtained by oxidative annealing.¹⁵⁴ The origin of this emission under reverse bias is thought to be a transition from an intrinsic shallow state (such as Zn_i) to an intrinsic deep state (such as oxygen vacancies in the ZnO). We note that the 640 nm emission intensity drops as the interface area between the ZnO backbone and GaN decreases. EL images at reverse bias show the light is mainly emitted from nanowires or nanowalls thus the e–h recombination is expected to occur in the ZnO layer.⁹⁶ Based on the energy of this emission at 1.95 eV, its origin is attributed to some mid-gap states in the ZnO. Under reverse bias, electrons from the GaN valence band can tunnel through the depletion region to this mid-gap state and descend to the ZnO valence band resulting in the observed orange emission. It is not clear how nitrogen and oxygen atoms are

arranged at the interface, thus the direction of charge transfer and the extent of the depletion of the ZnO/GaN interface is not clear.

As pointed out, the light collection and generation efficiencies in such heterojunctions are directly influenced by the concentration of charge carrier trap sites. The described 1D-heterostructures in comparison with popular thin film LED materials such as III-N family exhibit high quality junctions with substantially reduced defect populations and satisfactory optical properties. The device efficiency is also greatly influenced by the heat generation at the junctions, which is one of the current challenges in thin film LED industries,¹⁵⁵ and may be improved by the use of nanowire- and nanowall-based devices due to their larger surface areas and fin-like structures. Although further innovation in design is needed, 1D-nanosystems, benefiting from the rich material combinations and form factor diversity, are expected to offer new solutions as next generation LEDs both at the macro- and microscale.

4.2. Nanogenerators for harvesting mechanical energy

The vertically aligned nanowire morphology allows an entire array of nanowires to be connected in series *via* top and bottom contacts. This enables the integration of nanowire building blocks into large scale devices; one example of this is the recently developed nanogenerator (NG), which is a device that converts mechanical energy into electricity at the nanometre scale. The operating principle lies on the lateral deflection of piezoelectric nanowires, such as ZnO, which creates positive and negative piezoelectric potential on the tensile and compressive side surfaces, respectively. The NG is assembled by integrating a Pt-coated, serrated electrode with vertically aligned ZnO nanowires, and was demonstrated to convert ultrasonic waves into electricity.¹⁵⁶ As schematically shown in Fig. 24a, an array of aligned ZnO nanowires was grown on a GaN substrate and subsequently covered by a serrated Si electrode that had been coated with Pt. The Pt coating not only enhances the conductivity of the electrode, but also creates a Schottky contact at the interface with ZnO. The Schottky contact provides a built-in rectifying effect that only allows electrons to flow from the negatively-charged nanowires to the electrode (forward-biased connection) (Fig. 24b). The top electrode was composed of parallel serrated trenches fabricated on a (001) orientated Si wafer and coated with a thin layer of Pt (Fig. 24c). The electrode was placed above the nanowire arrays and manipulated by a probe station under an optical microscope to achieve precise positioning; the spacing was controlled by soft-polymer stripes deposited between the electrode and the nanowires at the four sides. A cross-sectional image of the packaged nanowire arrays is shown in Fig. 24d. Some nanowires were in direct contact with the top electrode, but some were located between the teeth of the electrode. Under the application of ultrasonic waves, the top electrode would move downward and impinge upon the nanowire leading to a lateral bending. The bending-induced piezoelectric potential would then be collected by the Pt film when the Schottky junction between the nanowire and Pt electrode was forward biased.

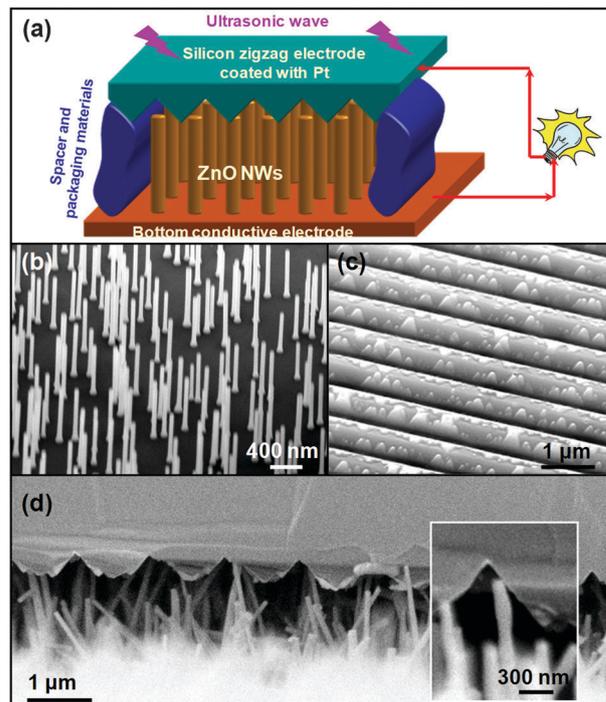


Fig. 24 Nanogenerators driven by an ultrasonic wave. (a) Schematic diagram showing the design and structure of the nanogenerator based on aligned ZnO nanowires. (b) Aligned ZnO nanowires grown on a GaN substrate. (c) Zigzag Pt-coated Si electrode with 200 nm of Pt. (d) Cross-sectional SEM image of the nanogenerator. Inset: A typical nanowire that is forced by the electrode to bend.

Due to the *in situ* rectifying effect of the Schottky contact, the detected output electrical signal exhibited a direct current (DC) characteristic. Although each nanowire would still produce electric pulses, accumulation of the output from all nanowire generated a constant DC current signal with large noises, as shown in Fig. 25a. The polarization of the DC signal is consistent with the bias direction of the Pt-ZnO Schottky barrier. When the connection of the electrical measurement system was switched between the two electrodes of the nanogenerator, the polarization of the output signal will be reversed accordingly but the signal amplitude is unaffected, as shown by the black curve in Fig. 25a. This phenomenon further proves the Schottky effect to the nanogenerator output and it is considered as a necessary condition to distinguish valid signals from measurement system artefacts.

The DC output of ultrasonic wave-driven nanogenerators allows for performance characterization by connecting a variable DC voltage source as the load, which is a condition similar to that of solar cell characterization. A typical J - V curve of a nanogenerator is shown in Fig. 25b demonstrating an open circuit voltage of ~ 10 mV and a short circuit current density of ~ 1 $\mu\text{A cm}^{-2}$, corresponding to an optimum output power of ~ 10 nW cm^{-2} . From the shape of the curve, the fill-factor (FF) was determined to be $\sim 25\%$. Thus the operational power of that particular nanogenerator was ~ 2.5 nW cm^{-2} . The low FF is likely associated with the large internal resistance due to a large number of branching nanowires and the poor contact

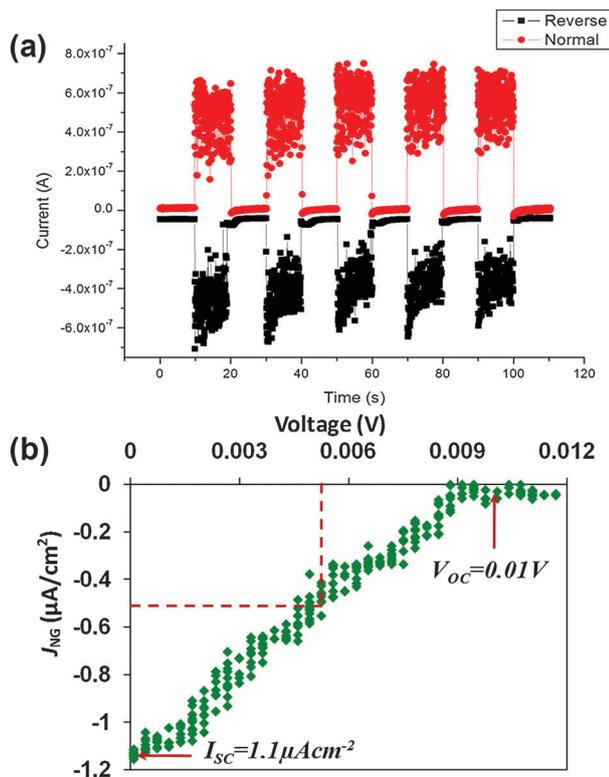


Fig. 25 (a) A typical DC current output of an ultrasonic-driven nanogenerator. (b) J - V curve of the nanowire during normal operation, where the short-circuit current and open-circuit voltage can be identified.

between nanowires and the Pt electrode. In an ideal case, if each nanowire is involved in the energy conversion process, the output power could be raised to the $\mu\text{W cm}^{-2}$ level. Most recently, by integrating a large number of ZnO nanowires in a single NG assembly, the output power has been significantly improved to the μW range and the voltage has been raised to ~ 2 V. The relatively high power is already sufficient to support the operation of small electronic devices, such as LEDs, LCDs and nanowire-based sensors.^{157–159}

Compared to conventional thin-film-based piezoelectric cantilever transducers, the use of piezoelectric nanowires for

mechanical energy scavenging offers three unique advantages. First, nanowires with a diameter of a few tens of nanometers or less exhibit an enhanced piezoelectric effect when subjected to a non-uniform strain. Secondly, the lattice perfection of nanowires enables much larger critical strain, higher flexibility, and longer operational lifetime. Finally, their large aspect ratio and small thickness allow the creation of significant strain in the nanowires under a force at the nanonewton or even piconewton level. Therefore, with the improvements in nanowire alignment and large-scale fabrication strategies, the NG will fundamentally improve the mechanical energy harvesting capability. This may eventually lead to an effective power source for self-powered electronic systems with higher energy density, higher efficiency, longer life time, as well as lower cost.¹⁶⁰

4.3. Photoelectrochemical electrodes (PEC)

High density tree-like 3D nanowire arrays can offer long optical paths for efficient light absorption, high quality one-dimensional (1D) conducting channels for rapid electron-hole separation and charge transport, as well as high surface areas for fast interfacial charge transfer and electrochemical reactions. Therefore, they are considered as an ideal architecture for high-performance PEC electrodes. Using a TiO_2 -Si heterogeneous 3D nanowire network, enhanced PEC efficiency for photocatalytic water splitting reactions was demonstrated.¹³⁶

Fabrication of 3D TiO_2 -Si nanowire architecture is schematically illustrated in Fig. 26a. First, vertical Si nanowire arrays were prepared by selectively etching a heavily-doped n-type Si substrate. Second, high density TiO_2 nanowires were uniformly grown around the Si nanowires *via* the SPCVD process. Lastly, an additional thin film of anatase TiO_2 was coated on the nanowire heterostructure by ALD to completely cover Si nanowire surfaces. As schematically shown in Fig. 26b, when this heterogeneous structure is used as a PEC anode for water splitting, photocatalyzed H_2O oxidation reactions would only occur on the TiO_2 surfaces. In principle, the photo-generated electrons should quickly be transported through the Si nanowire backbone and reach the counter electrode with minimal losses owing to the high conductivity of Si nanowires and isolation from the electrolyte. The very large surface area

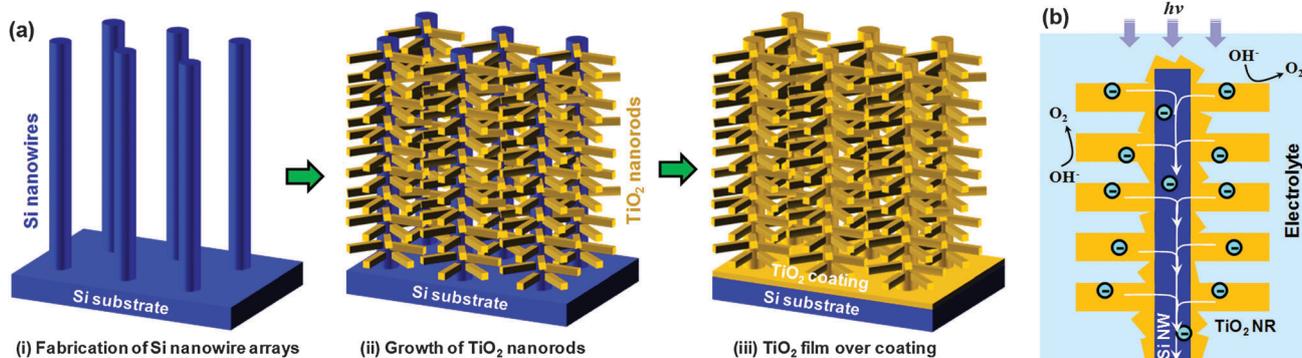


Fig. 26 (a) Schematic procedures for making treelike TiO_2 -Si nanowire 3D architectures. (b) Schematic illustration of using TiO_2 -Si nanowire heterostructure as PEC anodes for water splitting reactions.

provided by the TiO₂ nanowire arrays together with the high-speed electron transport channels provided by the Si nanowires are promising features that could lead toward a significant improvement of PEC efficiency.

The Si nanowire backbones were fabricated by either RIE dry-etching or metal-assisted wet-etching. The 3D nanowire network structure based on dry-etched Si nanowires has been shown in Fig. 18. High density TiO₂ nanowires were deposited on wet-etched Si nanowires. Fig. 27a is a planar view of a wet-etched Si nanowire forest after the growth of these nanowires. Closer examination showed that the Si nanowires were very thin and exhibited irregular cross sectional diameters as highlighted by yellow dashed circles in the inset of Fig. 27a. While the open spaces left within the bundling area were very small, the TiO₂ nanowires could be found filling all these spaces. These TiO₂ nanowires are 30 nm ± 6 nm in diameter and 243 nm ± 31 nm in length. Fig. 27b shows that the Si nanowires were ~25 μm in length, where the top portions (a few μm long) were bundled together. Below the bundles, Si nanowires are evenly distributed, providing a good template for conformal nanowires growth. Fig. 27(c-d) are two representative images indicating

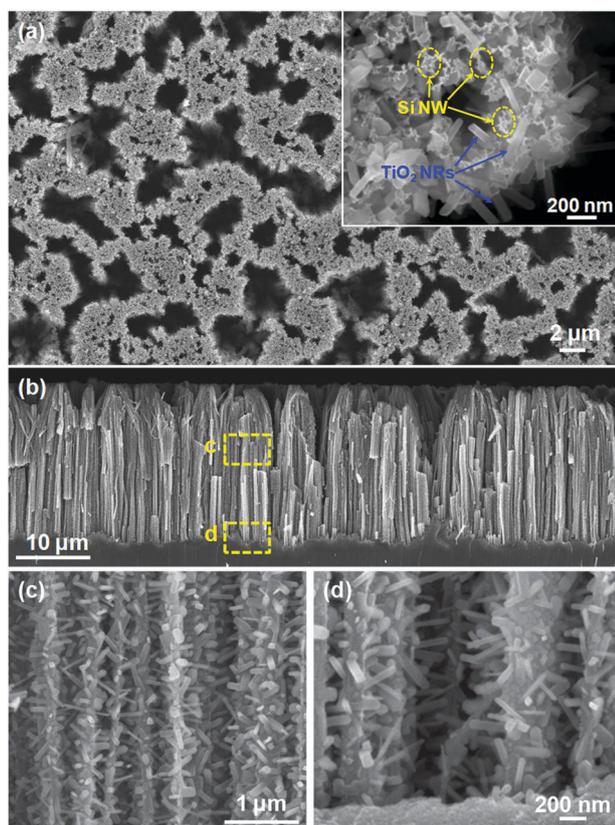


Fig. 27 TiO₂ nanowires grown on vertical Si nanowire arrays fabricated by wet etching. (a) Top view of Si nanowires after TiO₂ nanowire growth. Inset is a higher-magnification SEM image showing TiO₂ nanowires growing laterally around Si nanowires. (b) Cross-section of vertical Si nanowire arrays covered with TiO₂ nanowires. The Si nanowires are ~25 μm long and the top ~5 μm region was bundled together. (c,d) The middle and bottom portions of Si nanowires show dense and uniform coverage of TiO₂ nanowires along the entire nanowire length.

that the density and dimensions of TiO₂ nanowires were nearly identical at the middle and bottom regions. The nanowires grew laterally from the Si nanowires and filled out the interspaces. Thus, a structure exhibiting a considerably large surface area as well as high porosity was created by such a 3D architecture.

The TiO₂-Si nanowire 3D architectures were then used as a PEC anode for water oxidation in a 1 M KOH electrolyte using a three-electrode electrochemical cell configuration. Typical plots of photocurrent density *versus* bias potential are shown in Fig. 28a. The dark current density remained at a very low level (<10⁻² mA cm⁻²) under bias potentials between -1.2 V and 0.5 V (*vs.* SCE) indicating the high quality of the crystal surfaces of TiO₂. The merits of the 3D nanowire networks as PEC anodes were demonstrated by comparing the performance of three TiO₂-Si nanowire-based configurations. They are wet-etched Si nanowires with TiO₂ nanowires, dry-etched Si nanowires with TiO₂ nanowires, and wet-etched Si nanowires. All the Si nanowire templates were 10 μm long. The three plots followed the same trend and exhibited the same V_{OC} (open circuit voltage); while J_{SC} (short circuit current density) varied widely for these samples. The TiO₂ thin-film-coated Si nanowires produced a J_{SC} of ~0.66 mA cm⁻². Both nanowire coated samples exhibited significantly higher J_{SC} owing to their larger surface areas. Because the density of wet-etched Si nanowires was higher than that of dry-etched Si nanowires, it yielded the highest J_{SC} (~1.43 mA cm⁻²), which was more than twice that produced by the thin-film-coated sample.

The PEC performance was further investigated from various 3D nanowire geometries, including different Si nanowire lengths and thickness of TiO₂ over-coating (a necessary treatment in order to isolate Si from the electrolyte). From the resulting *J-V* curves, the PEC efficiencies were also evaluated *via* the equation:

$$\eta(\text{photo})\% = j_p(E_{\text{rev}}^0 - |E_{\text{bias}} - E_{\text{aoc}}|) \times 100/I_0 \quad (1)$$

where j_p is the photocurrent density, E_{rev}^0 is the standard state-reversible potential (1.23 V for water-splitting reaction), E_{bias} is the bias potential at which j_p is measured, and E_{aoc} is the bias potential at open circuit (-1.0 V when SCE and 1 M KOH electrolyte are applied). The calculated efficiencies of the TiO₂-Si 3D nanowire architectures were plotted as a function of biasing potential, as shown in Fig. 28b. Efficiency calculations showed that the 20 μm sample had an efficiency that was three times higher than the 1.5 μm sample, suggesting that the performance enhancement resulted from an increase in surface area. The highest efficiency (2.1%) was identified from the 20 μm sample with the 250-cycle over-coating. This value is >400% larger than the efficiency achieved by nanowire arrays without the branched structures. This comparison suggests that the 3D nanowire architecture is likely superior to straight nanowire arrays for PEC electrode design.

Using high-density 3D nanowire networks opens a new avenue toward high-performance electrode design, and could show substantial impacts on energy harvesting and storage devices. For example, V₂O₅ is widely investigated as a promising cathode material in lithium ion batteries.⁴⁴⁻⁴⁶ However, the

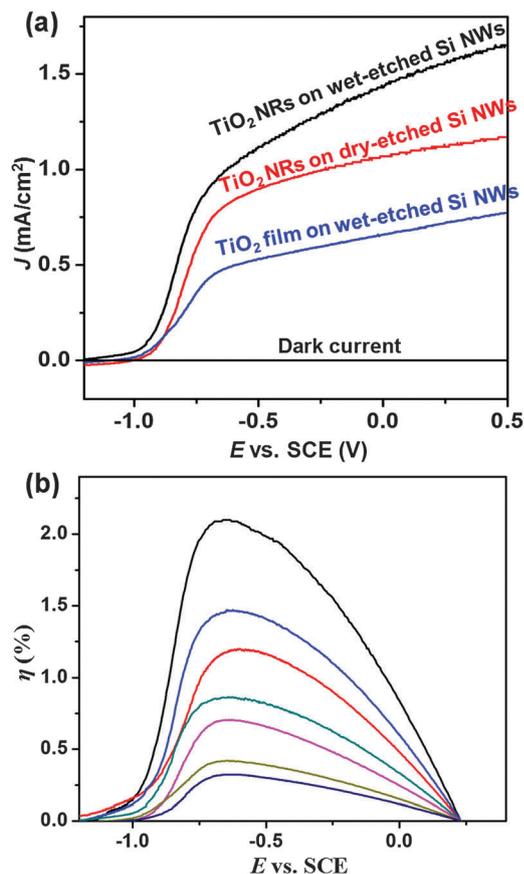


Fig. 28 (a) J - E curves and dark currents of different TiO_2 -Si nanowire (NR) configurations showing enhanced PEC performance by introducing high-density TiO_2 nanowire branches. (b) Efficiency vs. bias potential of different TiO_2 -Si nanowire configurations. The curves from top to bottom are measured from: $\text{TiO}_2/20 \mu\text{m}$ Si nanowire/250 cycles overcoating, $\text{TiO}_2/20 \mu\text{m}$ Si nanowire/375 cycles overcoating, $\text{TiO}_2/10 \mu\text{m}$ Si nanowire/205 cycles overcoating, $\text{TiO}_2/10 \mu\text{m}$ Si nanowire/375 cycles overcoating, $\text{TiO}_2/10 \mu\text{m}$ Si nanowire (dry etched)/375 cycles overcoating, $10 \mu\text{m}$ Si nanowire/375 cycles overcoating, and $\text{TiO}_2/1.5 \mu\text{m}$ Si nanowire/375 cycles overcoating, respectively.

poor electrical conductivity and low diffusion rate of Li^+ ions in V_2O_5 have stimulated the interest in nanowire morphologies which reduce the electron and ion diffusion length and enhance the power density. A 3D nanowire structure such as that presented in Fig. 26 is therefore ideal. The backbone nanowires are responsible for the high rate of charge transport, while the V_2O_5 nanowire branches are responsible for ion intercalation originating in the increased accommodations of transformational strain compared to their bulk counterpart. SPCVD is a powerful approach to producing this complex nanowire structure by choosing suitable precursors that do not decompose at high temperature. WO_3 ^{48–50} and Fe_2O_3 ^{51–53} are well-known photocatalysis materials due to their small band gaps, proper band alignments with water redox potentials and low cost. However, both materials are subject to short carrier diffusion length, resulting in very poor quantum efficiency. 3D nanowire structures are also beneficial to their catalytic applications since the charge collection efficiency and surface area could both be dramatically enhanced. With the

SPCVD approach, branched nanowires formed of WO_3 and Fe_2O_3 could be synthesized to escalate the surface area for efficient light absorption and surmount the charge transport problem *via* the highly-conductive backbone nanowires.

5. Conclusion

A detailed review on self-aligned and vapor-based growth of 1D-nanostructures of ZnO, TiO_2 and related materials is given. Some of the main demands of the nanotech industry in nanowire device integrations and applications are highlighted and limitations are discussed. Different growth mechanisms are explored and their advantages in interfacing nanowires to outside world are presented. The strength of the SVLS growth technique is in its high precision in controlling the hierarchy of nanowires and in large scale charge injection into planar arrays of 1D- or 2D-nanostructures. SPCVD technique offers a new capability to grow uniform nanowire branches inside high-density nanowire arrays. Understandings of these growth mechanisms and application potentials have led and will continuously lead to many new advancements for other functional nanomaterials, including WO_3 ,^{48–50} SnO_2 ,^{41–43,161} V_2O_5 ,^{44–46} and Fe_2O_3 ^{51,52} to name but a few. The high quality of the interfaces, well-controlled and aligned morphology, and extremely large surface area offers a high level of fidelity in their use in future nanotechnologies including electronic and optoelectronic devices, energy harvesting, conversion and storage systems.

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